Systematic Design Procedure for Q-Enhanced Integrated LC Filters

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***Abstract*— In this paper, we present a systematic design procedure for Q-enhanced integrated LC filters. It does not require any simulations and is thus suitable for design automation. The design procedure has been described in the CAIRO+ analog design environment, containing the BSIM3v3 models of the MOS transistor. Precise estimations of the quality factor and the resonance frequency were made possible by adding the integrated inductance π model into the design environment. Several design examples of 2.442GHz Q-enhanced LC filters are given in a 0.13 μm CMOS process.**

I. Introduction

Advances in highly integrated wireless communication transceivers provides potential applications for integrated RF bandpass filters. Active filters can achieve a high quality factor but with a poor dynamic range when operating at gigahertz frequencies. Passive LC filters can achieve high dynamic range at very low power consumption but requires high Q on-chip inductors.

Q-enhanced LC filters are a good compromise between these two types of filters [1]. Q-enhanced LC filters are not only used to realize integrated RF bandpass filters [2] but they are also used in the design of RF bandpass $\Sigma\Delta$ modulators [3].

Fig.1 shows a simple and popular realization of a Q-enhanced LC filter using a differential negative resistor. The design of such a circuit usually requires a significant amount of iterations with a SPICE-like circuit simulator. This is due to the fact that manual design equations are based on the parallel RLC inductor model, shown in Fig.1, while on-chip inductors models in circuit simulators are usually based on the more elaborate π model [4], shown in Fig.2.

In this work, we propose a systematic design procedure for Q-enhanced LC filter that does not require any iterations with a circuit simulator. The idea is to calculate, in the design phase, the quality factor and the resonance frequency of the LC filter using the π model for the inductor and the BSIM3v3 models for the transistors. The design procedure is described in the analog design environment CAIRO+ [5].

In section II, we present the procedure used to size the transistors of the negative resistance based on the estimation of the quality factor of the original lossy LC tank. In section III, we show how the resonance frequency is adjusted based on a relation based on the π model and accurate estimation of the transistors parasitic capacitances. The complete design automation procedure is presented in section IV. Comparisons between predicted performances and simulation results for several design examples are given in section V.

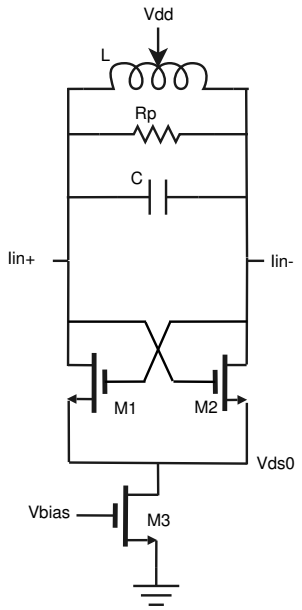

Fig. 1. Q-enhanced LC filter with differential negative resistance.

II. Quality Factor Enhancement

Due to its nature, an integrated inductor presents some parasitics resistances and capacitances. Resistances are due to intrinsic resistance of the employed metal and interconnect and skin effect at high frequencies, and lossy substrate. The inductor with these parasitics can be modeled by the π model Fig.2. As shown in Fig.3, we approximate this π model with a RLC model for a certain range of frequency, for example the desired central frequency of the filter. In this case we take:

$$R_{pL} \approx \frac{R_s}{(\omega_0 L)^2} \qquad R_{pC} \approx \frac{1}{R_{sub}(C_{sub}\omega_0)^2}$$

$$R_p = R_{pL} // R_{pC} \tag{1}$$

Then we can replace the π model by a RLC bridge with a R_p resistor, a C_{sub} capacitor and L inductor. Once we have a value for a parallel resistor, we can obtain a value for the quality factor of the inductor by:

$$Q_0 = \frac{L\omega_0^2}{R_p} \tag{2}$$

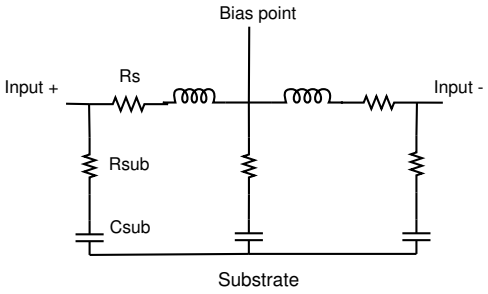

Fig. 2. Simplified π model for a differential center-tapped spiral inductor.

Using the differential negative resistance circuit shown in Fig.1, the quality factor is now equal to:

$$Q_{enh} = \frac{Q_0}{1 - Gm_0 R_p} \tag{3}$$

So choosing an appropriate value for Gm_0 can improve the value of the quality factor of the original lossy LC tank from Q_0 to a desired quality factor Q_{enh}.
Gm_0 is the equivalent transconductance of the differential negative resistance, and is equal to:

$$Gm_0 = Gm - Gds \tag{4}$$

where Gm and Gds are respectively the transconductance and the output conductance of transistor M1. In the CAIRO+ analog design environment, it is possible to perform an accurate sizing of a transistor in order to obtain a certain transconductance Gm. Once we have the dimensions of the transistor, it is also possible to extract the precise value of Gds. A few iterations are then required to size transistors M1 and M2 according to the required overall Gm_0 of the differential negative resistance.

III. Resonance frequency

As will be shown later in section V, the approximation by a parallel resistor is sufficiently accurate for the quality factor calculations. Unfortunately, it is not the case for the resonance frequency calculations. In Fig.4, we plot the total impedance calculated with the parallel and the series resistor versus frequency. We can see with the series resistor, the resonance frequency in shifted by 10 Mhz from the standart $\omega_0 = 1/\sqrt{LC}$ value. Using a series resistor model, the total impedance is:

$$Z(j\omega) = \frac{(-1/Gm_0)(Rs + j\omega C)}{-j\omega C(Rs + j\omega L)/Gm_0 + Rs + j\omega L - 1/Gm_0} \tag{5}$$

It is difficult to obtain an analytical expression for resonance frequency from this formula. A numerical method is used to compute the required capacitor value for a desired resonance frequency. This procedure gives us a value: C_{total} for the total capacitance at the input node. In order to adjust the resonance frequency of the filter, the total parasitic capacitances, C_{par}

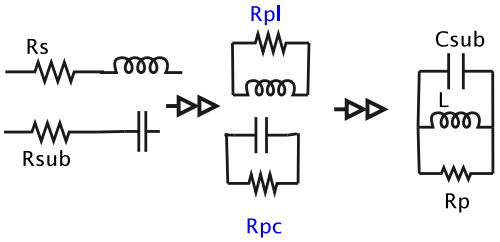

Fig. 3. pi model to parallel model transformation.

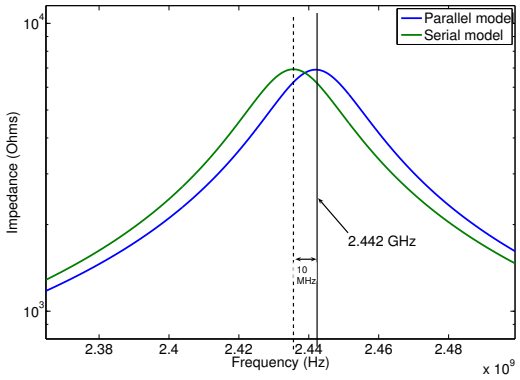

Fig. 4. Resonance frequency shift due to approximating losses by a parallel resistor, $Q_{enh} = 60$, $F_0 = 2.442$ GHz, $R_s = 10\Omega$

due to the inductor and the transistors have to be taken into account:

$$C_{par} = C_{sub} + Cdg + Cgd + Cgs + Cds \tag{6}$$

The MOS parasitic capacitances are easily obtained, using the BSIM3v3 model. C_{sub} is obtained from the inductor pi model. Both models are embedded in the CAIRO+ design environment.

IV. Design Automation and Characterisation

A. CAIRO+ Design Environment

CAIRO+[1], is a framework, developed at the LIP6 laboratory, which aims at helping analog circuit designers to automate the design of their circuits [6]. It provides a library of functions to describe the netlist template, layout template, specification template, design space exploration procedure and layout generation. The general method in CAIRO is to design Modules using devices. Each module has a list of defined parameters, and one or more procedure.
In our case, the goal is to design a bandpass Q-enhanced LC filter. The input parameters are: the desired quality factor, the resonance frequency, the input bias, and the value of the inductor with its geometrical parameters. The procedure will calculate and returns the sizes of the transistors, and the value of the capacitor of the resonnator. A flowchart of the proposed design procedure, described in section II and III, is illustrated in Fig.5

[1]CAIRO stands for: "Optimized and Reusable Integrated Analog Circuits" in French.

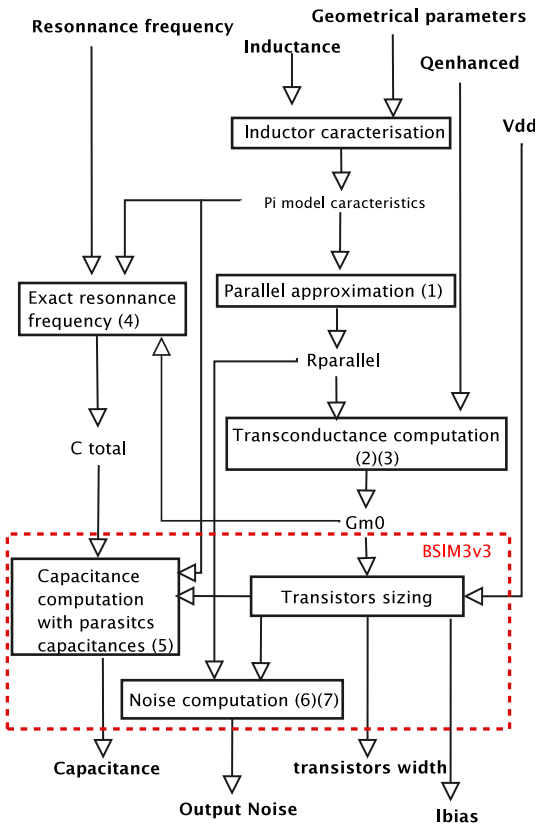

Fig. 5. Q-enhanced LC filter design procedure.

B. Noise Characterization

Noise performance is an important characteristic of the designed Q-enhanced LC filter. We have also implemented a method to compute the noise generated by the filter. The noise sources in the circuit are represented in Fig.6. The thermal noise generated by transistors ($\overline{In_M^2}$) is computed using Cairo's transistor device, which include a procedure to compute thermal noise. The thermal noise of the resonnator is computed using the total parallel resistor as approximated in **??** so:

$$\overline{In_R^2} = \frac{4k_BT}{R_p} \tag{7}$$

We have two current noise sources, we add the two spectral noise density to obtain the total current noise spectral density at the input. We can compute the equivalent voltage noise at the output by multiplying it by the total gain (the total impedance at the given frequency of the filter) and integrate it over the useful bandwidth (BW) to have the output noise power :

$$P_n = \int_{BW} |Z(\omega)|^2 (\overline{In_R^2} + \overline{In_M^2}) df \tag{8}$$

V. Simulation Results

Once the filter is sized, we can export a netlist file, which can be simulated. Here are the results of those simulations.

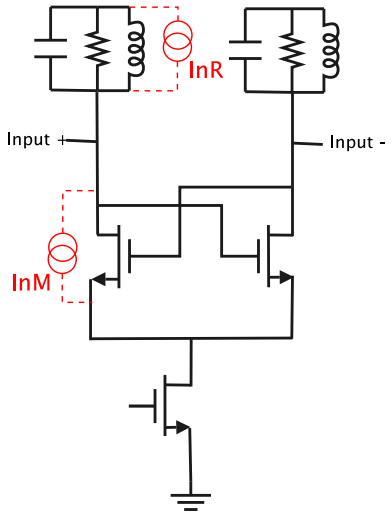

Fig. 6. Noise sources in the filter

A. Quality factor and resonance frequency

In Fig.7 we plot the impedance versus input frequency for several values of Q. this way we could measures effective Q and resonance frequency. The parameters are: resonance frequency : 2.442 GHz, 5 nH inductor (4 turns, 12 μm width and 10 μm spacing, which give a $Q_0 = 15$) for a 0.13 μm technology. The bias conditions are : Vin = 0.6V, Vds0 = 0.3V. As we can see, the automatic design procedure is precise for the effective quality factor and the frequency.

B. Linearity

One fact this work has permit to underline is the importance of input bias voltage on linearity. As it is easy to generate filter sized to work with different input bias, we studied the linearity of those filters by plotting the output power versus input power in Fig.8(Vds0 stays at 0.3V). We also studied the intermodulation (IM3) with a two-tones signal. In Fig.9, we can see that the input voltage bias has a strong influence on the 1dB compression point.

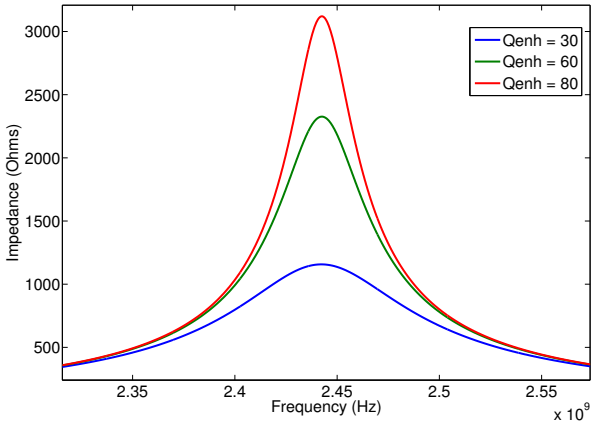

Fig. 7. Total impedance for different values of Q

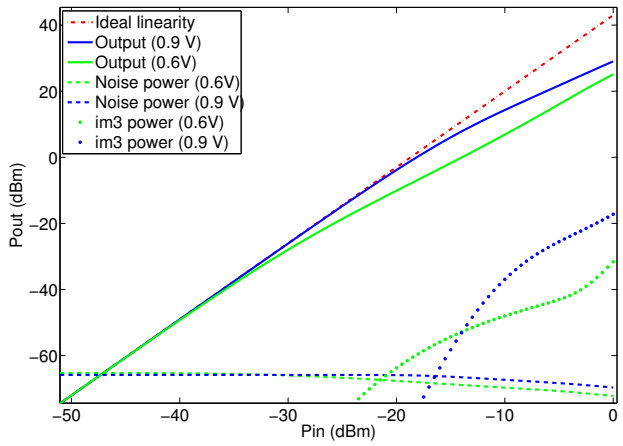

Fig. 8. Output Signal, Output noise floor and IM3 versus Input power for different values of inductor biasing voltage, V_{dd}.

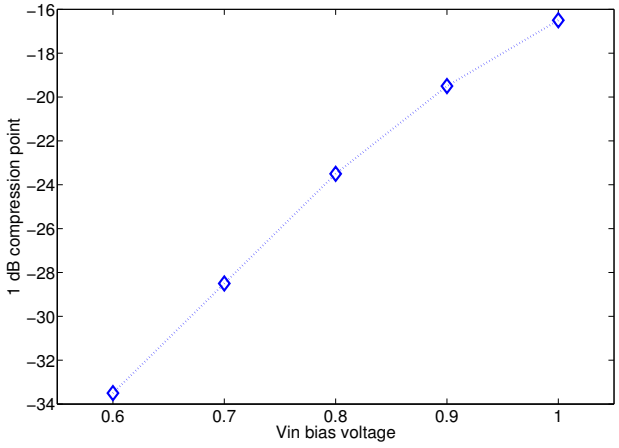

Fig. 9. 1 dB compression point versus inductor biasing voltage, V_{dd}.

TABLE I

COMPARISON BETWEEN CAIRO AND SIMULATION RESULTS.

CAIRO			Simulation		
f_0 (GHz)	Q	P_n (dBm)	f_0 (GHz)	Q	P_n (dBm)
2.442	30	-69.0	2.4423	30.29	-67.0
2.442	60	-65.0	2.4425	60.28	-63.0
2.442	80	-63.5	2.4425	81.30	-61.5
2.442	100	-62.5	2.4426	101.6	-60.5

TABLE II

PERFORMANCES OF A GENERATED Q-ENHANCED LC FILTER COMPARED WITH SOME OTHER RECENT DESIGNS.

	f_0	Q	1dB DR	P_{dc}	FOM
This Work	2.442 GHz	80	32	**0.65 mW**	118.8
[7]	2.12 GHz	31	59.6	143 mW	119.2
[8]	900 MHz	45	61.5	39 mW	120.5
[9]	2.1 GHz	40	37.6	5.2mW	109.8

C. Comparison with other works

A figure of merit to caracterize the Dynamic Range of a filter, taking power consumption into account, is proposed in [8]:

$$FOM = \frac{P_{1dB}}{P_{noise\,1Hz}\ P_{dc}} \tag{9}$$

where $P_{noise\ 1Hz}$ is the output noise power spectral density in 1 Hz bandwidth. In our case we take the power density at the central frequency of the filter, and P_{dc} is the power consumption of the filter. In table II, we compare the performance of a filter generated using our design procedure with some other recent designs.

VI. CONCLUSION

In this paper, we have presented a systematic design procedure for Q-enhanced LC filters. The procedure is based upon the inductor π model and the BSIM3v3 transistors' model. It has been shown that a parallel RLC model is sufficient to calculate the required transconductance of the differential negative resistance. On the other hand, a series model for the inductances losses is necessary for precise calculation of the resonance frequency. Several design examples have been presented to demonstrate the validity of the approach. Very little difference has been observed between the estimated performances of the circuits generated using the proposed design procedure and the performances measured from simulation.

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