Design of Continuous-Time $\Sigma\Delta$ Modulators with Sine-Shaped Feedback DACs

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***Abstract*— This work presents a general method to design continuous-time $\Sigma\Delta$ modulators with sine-shaped feedback DACs. A discrete time to continuous time transformation technique is used to compute the continuous-time loop filter coefficients, taking into account the sinusoidal feedback. Examples of high order lowpass and bandpass continuous-time $\Sigma\Delta$ modulators are given as an illustration for the proposed design method. A transistor level sine-shaped feedback DAC is also proposed and compared to a recent circuit design. Finally, the sensitivity of these circuits to clock jitter is studied and compared to the traditional rectangular feedback pulse.**

I. Introduction

Continuous-Time (CT) Sigma-Delta modulators have received a significant interest in the recent years due to some important advantages over their Discrete-Time (DT) equivalents. Intrinsic anti-aliasing filter, lower thermal noise and higher sampling rate make these modulators more suitable for low-power or high-speed applications and commonly used for analog to digital conversion in radio receivers [1].

The main drawback of CT $\Sigma\Delta$ modulators is their high sensitivity to any non-idealities in the feedback path. Clock jitter is probably the major imperfection that can significantly degrade the performance of high speed CT $\Sigma\Delta$ modulators.

Most of the actual CT $\Sigma\Delta$ modulators are based on rectangular feedback schemes (NRZ, RZ) which are quite easy to design and work properly for intermediate sampling frequencies. However, as sampling rates are getting higher and higher, rectangular feebacks tend to look more like sinusoidal ones, which forces the designer to review the design procedure of these CT $\Sigma\Delta$ modulators. Furthermore, recent theoretical work on sine-shaped feedbacks has proven that they are less sensitive to clock jitter compared to rectangular feedbacks [2].

In this paper, we present a general method for designing an n^{th} order CT $\Sigma\Delta$ modulator with a sine-shaped feedback DAC. This method is valid for the different lowpass and bandpass topologies.

In Section II, we describe the procedure we have followed to compute the CT loop filter coefficients. Section III gives some design examples of lowpass and bandpass CT $\Sigma\Delta$ modulators using sine-shaped feedbacks. Section IV discusses some circuit design issues and conclusions about this work are drawn in Section V.

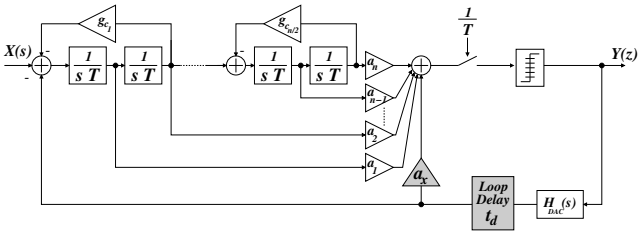

Fig. 1. Continuous-time $\Sigma\Delta$ modulator with loop delay, t_d, and feedback compensation coefficient, a_x.

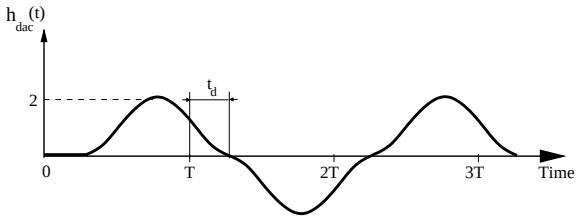

Fig. 2. Delayed sine-shaped feedback signal, $h_{dac}(t) = 1 - \cos(\omega t)$.

II. Loop Filter Coefficients for Sine-Shaped Feedbacks

The continuous time loop filter coefficients are calculated using a DT-to-CT transformation technique [3], which consists of equating the loop gains for both discrete and continuous time modulators. To design the CT $\Sigma\Delta$ modulator, we will therefore start from the DT loop filter coefficients and then establish the DT-to-CT equivalence.

Fig. 1 shows a general form of a CT $\Sigma\Delta$ modulator with feedback loop delay. The objective is to design the CT loop filter $H_c(s)$ for the proposed feedback DAC transfer function $H_{DAC}(s)$, so that the CT $\Sigma\Delta$ sampled loop gain $G_c(z)$ is equal to the DT $\Sigma\Delta$ loop gain $G_d(z)$. This can be expressed by :

$$\begin{aligned} G_d(z) &= G_c(z) \\ H_d(z) &= \mathcal{Z}\left[\left(H_c(s) - a_x\right) H_{DAC}(s)\right] \end{aligned} \quad (1)$$

where $H_d(z)$ is the DT loop filter and a_x is an extra feedback coefficient added to compensate for the loop-delay [4] [5]. Notice that this compensation technique remains valid for feedback delays up to one clock period.

We will start by calculating the feedback DAC transfer function, then we will show the systematic design procedure

that we have followed to find the CT $\Sigma\Delta$ cofficients.

A. Feedback DAC transfer function

The feedback signal for a sine-shaped DAC is shown Fig. 2. We propose here to model the DAC logic circuitry delay and any additionnal settling times in the feedback path as a total delay t_d. The feedback DAC time response is then given by:

$$h_{DAC}(t) = [1 - \cos\,(\omega(t - t_d))]\,[u(t - t_d) - u(t - t_d - T)]$$

where $\omega = \frac{2\pi n}{T}$, *n* being the desired number of sine pulses per sampling period, T. Notice that the *n* parameter can take any real value, but for jitter sensitivity reasons, it should be kept to an integer value.

In the following study, we will suppose that the total feedback delay never exceeds one clock period. Applying the Laplace Transform to the time response, we get the following feedback DAC transfer function :

$$H_{DAC}(s) = \mathcal{L}[h_{DAC}(t)] = \frac{\omega^2(1 - e^{-Ts})e^{-t_d s}}{s(s^2 + \omega^2)}$$

The presence of the $e^{-t_d s}$ term in the H_{DAC} transfer function will require the use of the *modified-z-transform* technique [6] to solve equation (1). While avoiding the complex mathematics necessary to perform time-domain convolution, this technique enables us to get the *z*-transform of signals having variations between two sampling instants.

B. Modified z-transform

The loop gain transfer function of a CT $\Sigma\Delta$ modulator with a delayed sine-shaped feedback can be written in the following form:

$$G_c(z) = \mathcal{Z}\left[(H_c(s) - a_x)\,\frac{\omega^2(1 - e^{-Ts})e^{-t_d s}}{s(s^2 + \omega^2)}\right]$$

Using the modified-*z*-transform, we get:

$$G_c(z) = (1 - z^{-1})\mathcal{Z}_m\left[(H_c(s) - a_x)\,\frac{\omega^2}{s(s^2 + \omega^2)}\right]$$

where $m = 1 - \frac{t_d}{T}$.

To calculate the modified-*z*-transform of the CT $\Sigma\Delta$ loop gain starting from the Laplace domain, we use the *Residue theorem* [6]. $G_c(z)$ can then be written in the following form:

$$G_c(z) = (1 - z^{-1})\sum_{p_i} \text{Residues of } \frac{(H_c(s) - a_x)\omega^2}{s(s^2 + \omega^2)}\frac{e^{mTs}}{z - e^{Ts}}\Bigg|_{p_i} \quad (2)$$

where:

$$p_i = \text{poles of } \frac{H_c(s) - a_x}{s(s^2 + \omega^2)}$$

Using equation (2), the loop gain of the CT $\Sigma\Delta$ can be expressed in the DT domain. Comparing the coefficients of the numerator and the denominator of $G_c(z)$ with those of the DT loop gain $G_d(z)$, we should then be able to deduce the coefficients of the CT loop filter $H_c(s)$.

We take here the example of a 2^{nd} order bandpass CRFF CT $\Sigma\Delta$ modulator, where (g_{d_1}, b_1, b_2) are the DT loop filter coefficients and (g_{c_1}, a_1, a_2) are the CT loop filter coefficients. Implementing the DT-to-CT transformation using the symbolic mathematical tool MAPLE [7], equation (1) becomes :

$$G_d(z) = G_c(z)$$

$$\frac{(b_1 + b_2)z - b_1}{z^2 + (g_{d_1} - 2)z + 1} = \frac{\alpha_2 z^2 + \alpha_1 z + \alpha_0}{z(\beta_2 z^2 + \beta_1 z + \beta_0)}$$

where :

$$\alpha_i, \beta_j = f(a_1, a_2, a_x, g_{c_1}, t_d) \qquad (i, j) \in \{0, 1, 2\}$$

By cancelling the α_0 term with the appropriate a_x value, we get an expression for the CT loop gain $G_c(z)$ having the same order as the DT loop gain $G_d(z)$. The equivalence is thus established and we can compute the CT loop filter coefficients. Using MAPLE, we get for the 2^{nd} order CRFF CT modulator:

$$\begin{cases} g_{c_1} = (\pi - \arccos(-1 + \frac{g_{d_1}}{2}))^2 \\ a_1, a_2 = f(b_1, b_2, t_d) \\ a_x = f(a_1, a_2, g_{c_1}, t_d) \end{cases}$$

In the following section, we will show some design examples of high order CT $\Sigma\Delta$ modulators with delayed sine-shaped feedbacks.

III. Design Examples

Here we present a 5^{th} order lowpass CIFF and a 4^{th} order bandpass CRFF $\Sigma\Delta$ modulators. A sine-shaped feedback DAC with a total delay of $t_d = 0.625 * T$ is used within the CT modulators.

The DT $\Sigma\Delta$ loop filter coefficients have been obtained using Schreier's $\Sigma\Delta$ Toolbox [8]. Using the design procedure presented in the previous section, the CT $\Sigma\Delta$ coefficients were then obtained for a sine-shaped feedback.

The coefficients of the DT, CT with a feedback of one cycle per period (n=1) and CT with a feedback of three cycles per period (n=3) are listed in Table I for a 4^{th} order CRFF bandpass modulator.

Fig. 3 and Fig. 4 show the Signal-to-Noise Ratio resulting from the simulation of the DT modulators and the CT modulators with sine-shaped feedback DAC (n=1 and n=3).

We clearly see that the performances of the CT $\Sigma\Delta$ modulators with sine-shaped feedback are very close to the performances of the equivalent DT modulators.

TABLE I

4^{th} ORDER BANDPASS CRFF $\Sigma\Delta$ COEFFICIENTS (f_0=0.25f_s, OSR=64).

DT		CT	n = 1	n = 3
b_1	0.5587	a_1	-0.13246	-0.13144
b_2	-0.5587	a_2	-1.11473	-1.18358
b_3	-0.0158	a_3	-0.34010	-0.36064
b_4	-0.1999	a_4	0.15810	0.16765
g_{d_1}	1.9717	g_{c_1}	2.42314	2.42314
g_{d_2}	2.0283	g_{c_2}	2.51205	2.51205
		a_x	-0.03783	-0.42679

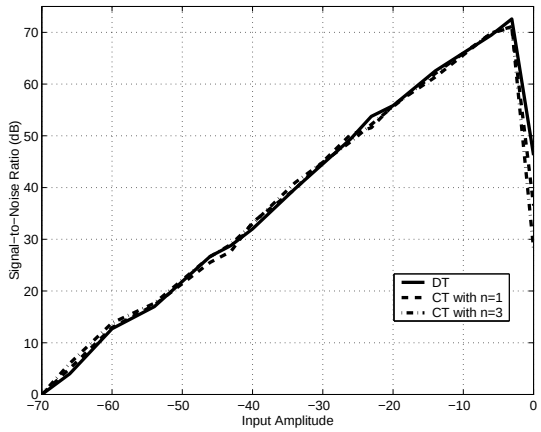

Fig. 3. Fourth order bandpass CRFF (f_0=0.25f_s, OSR=64).

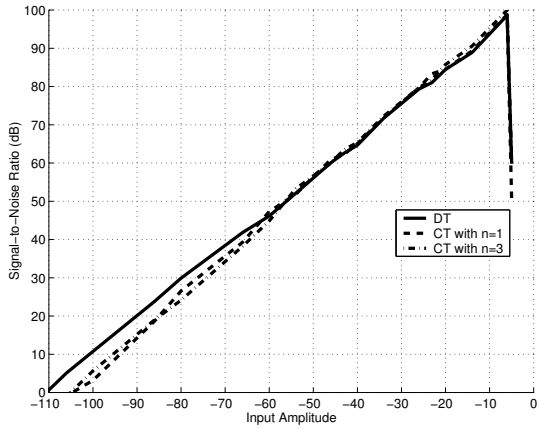

Fig. 4. Fifth order lowpass CIFF (OSR=64).

IV. Circuit Design Issues

We present here a sinusoidal feedback DAC for CT $\Sigma\Delta$ modulators with high sampling frequencies and compare it to the sine-shaped DAC proposed in [9]. Advantages and drawbacks of both designs will be listed and clock jitter effects will also be discussed.

A. Referenced sine-shaped DAC

In [9], the authors present a sine-shaped feedback DAC for CT $\Sigma\Delta$ modulators. The circuit is based on a current source controlled by a local oscillator, as depicted in Fig. 5. In the ideal case, the sine-shaped feedback pulses are perfectly locked to the DAC clock. Data switching occurs then at zero values of the output current, which has the benefit of considerably decreasing the clock jitter effects.

Since the input data and the oscillating waveform must be locked to the DAC clock, the use of additionnal synchronisation blocks and eventually a phase-locked loop might be necessary.

B. Proposed sine-shaped DAC

The proposed sine-shaped feedback DAC is shown Fig. 6. The circuit was designed using a 0.13μ CMOS technology.

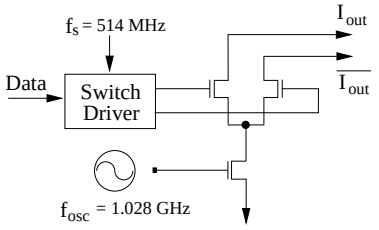

Fig. 5. Sinusoidal feedback DAC presented in [9], implemented in 1.8-V 0.18-μm CMOS technology.

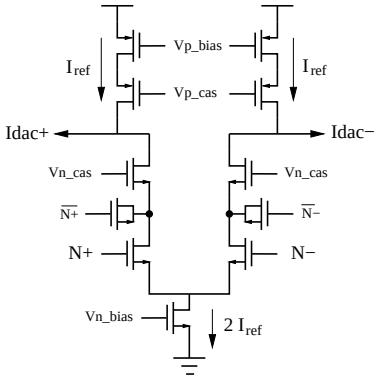

Fig. 6. Proposed sine-shaped feedback DAC, designed in 1.2-V 0.13-μm CMOS technology, f_s=9.768GHz.

Power dissipation is 1.2 mW with a 1.2-V supply voltage.

During return to zero, both switches N+ and N- are on and steer a current $-I_{ref}$ each, which compensates for the constant P source current $+I_{ref}$ and cancels the value of the resulting output current. During the next phase and depending on the input data, only one of the two switches remains on and steers all the N source current $-2I_{ref}$.

For sampling frequencies below 5 GHz, rectangular return to zero current pulses are generated at the outputs, but with higher sampling rates the output signals become nearly sinusoidal.

The output currents, for a sampling frequency of 9.768 GHz and for a constant '1' at the input, are shown Fig. 7. The total feedback delay was estimated here at a value of $t_d = 0.625{*}T$. This delay is mainly due to the response time and switching transitions of the logic gates within the control circuitry.

Compared to the referenced DAC [9], we are not concerned here by the synchronisation of the input data with the DAC clock, as long as the quantizer response-time doesn't exceed half a sample period (return to zero phase).

On the other hand, the proposed architecture is more subject to clock jitter, as it will be explained in the following subsection.

C. Analysis of Timing Jitter

In [2], the theoretical SNR limit due to clock jitter for the sine-shaped feedback is given by:

$$SNR = 20\log_{10}\left(\frac{\alpha}{\sqrt{2}}\frac{\sqrt{OSR}}{3.65\,\pi^2\,f_s^3\,\sigma_t^3}\right) \qquad (3)$$

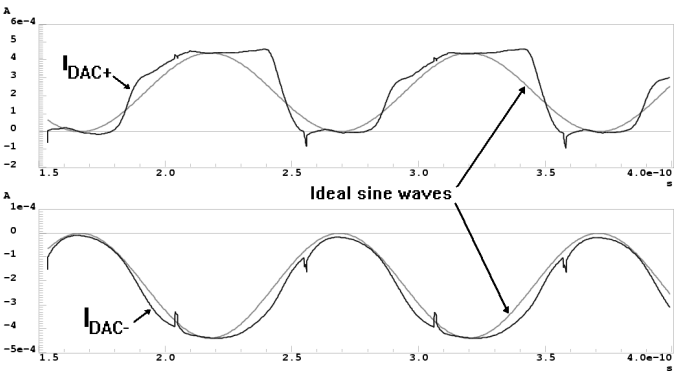

Fig. 7. Output currents of the proposed DAC (Fig. 6) at f_s = 9.768 GHz.

where σ_t is the clock jitter standard deviation and α is the input sine amplitude.

On the other hand, SNR limitation for a rectangular return-to-zero feedback with $\frac{T}{2}$ pulse width is, [10] :

$$SNR = 20\log_{10}\left(\frac{\alpha}{\sqrt{2}}\frac{\sqrt{OSR}}{2\,f_s\,\sigma_t}\right) \tag{4}$$

Fig. 8 shows the SNR of a 4^{th} order bandpass CRFF $\Sigma\Delta$ with OSR=58 and α=0.5 in function of the clock jitter (% of sampling period). The three plotted curves correspond to:

- SNR with jitter noise from (3) plus quantization noise
- SNR simulation results using ideal models for the loop filter and quantizer, and a transistor level netlist for the proposed feedback DAC (Fig. 6). Simulations were performed by injecting clock jitter only at half periods ($\frac{mT}{2} \pm \delta t$) and by keeping the sampling times at values of mT.
- SNR with jitter noise from (4) plus quantization noise.

The SNR degradation of the proposed circuit compared to the ideal sine shaped DAC lies in the way the jitter affects the feedback signal. In [2], the DAC is designed in a manner that the jitter affects the feedback signal only at the sampling instants (zero value and zero slope of I_{DAC}). Whereas, for our sine-shaped DAC, the jitter intervenes also at half periods, as depicted in Fig. 9.

V. Conclusion

In this paper, we have presented a general method to calculate the loop filter coefficients for CT $\Sigma\Delta$ modulators with a sinusoidal feedback. The design procedure has been validated through examples of high order lowpass and bandpass CT $\Sigma\Delta$ modulators. A sine-shaped DAC has also been proposed and compared to a recent work on sinusoidal feedbacks. Although the proposed design is more sensitive to clock jitter, it does not require the use of synchronisation circuitry.

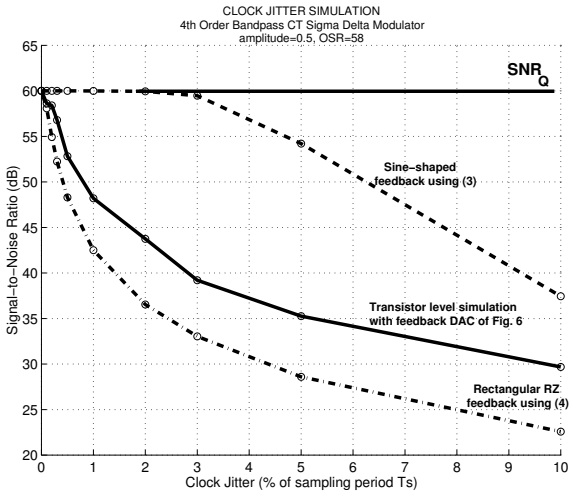

Fig. 8. Comparison of jitter-limited SNR for CT $\Sigma\Delta$ modulators using, the proposed feedback DAC, a rectangular return-to-zero DAC, and the sine-shaped DAC developed in [2].

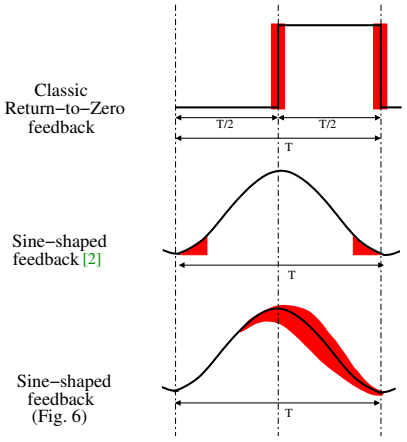

Fig. 9. Jitter effects for the three studied cases.

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