Jitter Analysis of Bandpass Continuous-Time ΣΔMs for Different Feedback DAC Shapes

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***Abstract*—In this paper, a simple and intuitive technique for analyzing clock jitter effect on bandpass Continuous-Time Sigma-Delta (ΣΔ) modulators is introduced. The power spectral density of the jitter noise for different feedback DAC shapes are derived and compared. It is shown that DAC output signal shapes used to reduce clock jitter sensitivity in lowpass Continuous-Time ΣΔ modulators may not be suitable for bandpass modulators.**

I. Introduction

Continuous-Time (CT) Sigma-Delta Modulators (ΣΔMs) are receiving more and more attention due to their advantages compared to Discrete-Time (DT) ΣΔMs. Inherent anti-aliasing filtering, lower thermal noise, higher sampling rate and lower power consumption are all attractive advantages of CT ΣΔMs that make them interesting solutions for high data-rate wireless communication systems [1]. Bandpass CT ΣΔMs are considered a promising technique for realizing software defined radio (SDR), as they can achieve a reasonable dynamic range by converting only the band of interest around the desired center frequency. Thus, the direct digitization of the RF signal is possible and almost all the signal processing can be done in the flexible and programmable digital domain [2] .

The main disadvantage of CT ΣΔMs is their sensitivity to the clock jitter of the feedback Digital-to-Analog Converter (DAC). The clock jitter noise of the feedback DAC is not shaped by the loop filter, due to its direct connection to the input node. It appears as a white noise in the signal band, and causes a degradation in the Signal-to-Noise-Ratio (SNR) of the modulator [3]–[5]. The feedback DAC output waveform can be shaped to reduce the jitter effect by using a sine shaped (Sine) DAC as in [1], [6], or by using a Switched-Capacitor (SC) DAC as in [7], [8].

The publications discussed the clock jitter effects in CT ΣΔMs are either limited to lowpass CT ΣΔMs as in [4], or limited to rectangular feedback DACs as in [9]. In this work, we introduce a simple and generic approach to analyze the clock jitter in both lowpass and bandpass CT ΣΔMs with different types of feedback DACs. The effect of clock jitter of feedback DAC is modeled as an additive noise [3], [10], as shown in Fig. 1, where the jittered DAC output is replaced with an ideal DAC output added to a jitter noise.

The jitter analysis for each feedback DAC type is done using three main steps. The first analysis step is to calculate the jitter noise of the feedback DAC, which is defined as:

$$j(t) = h_j(t) - h(t) \tag{1}$$

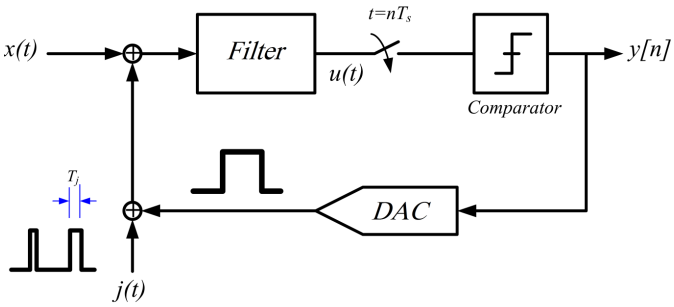

Fig. 1. Modeling clock jitter effect as an additive noise.

where $h_j(t)$ is the jittered DAC pulse, and $h(t)$ is the ideal DAC pulse. The calculated jitter noise may need some approximations to facilitate the next analysis steps. The second analysis step is to calculate the autocorrelation of the jitter noise using [11]:

$$R_j(\tau) = \frac{1}{T}\int_0^T j(t)\, j(t+\tau)\, dt \tag{2}$$

where T is the sampling time of the modulator. The last analysis step is to calculate the power spectral density of the jitter noise using Fourier Transform [11]:

$$S_j(f) = F\{R_j(\tau)\} = \int_{-\infty}^{\infty} R_j(\tau)\, e^{-2j\pi f\tau}\, d\tau \tag{3}$$

The power spectral density of the jitter noise is a good measure of the jitter performance, and can be used as a comparison metric between the different feedback DACs types. For a fair comparison, the pulse amplitude of each feedback DAC type is chosen such that the pulse area is approximately the same as the NRZ pulse:

$$\int_0^T h(t)\, dt \simeq T \tag{4}$$

II. Rectangular NRZ DAC

Rectangular NRZ DAC is the simplest type of DACs. The output of the DAC switches between two voltages levels corresponding to logic '1' and logic '0' of the modulator output. Applying (1) to NRZ DAC, the jitter noise is obtained as shown in Fig. 2(b, c, d). As the width of the jitter noise pulse

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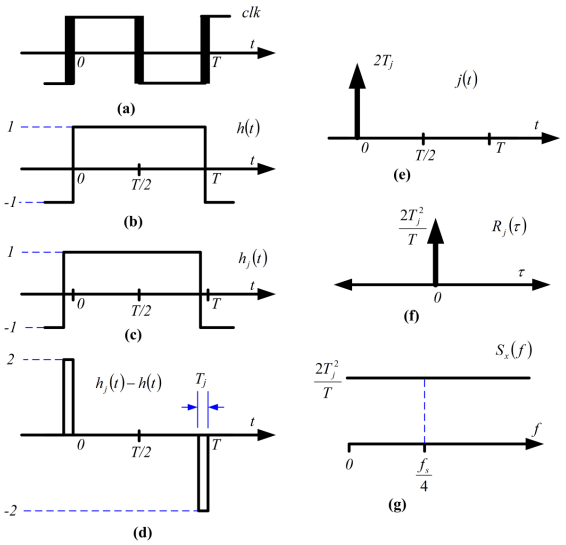

Fig. 2. NRZ DAC jitter (a) Clock. (b) Ideal DAC pulse. (c) Jittered DAC pulse. (d) Jitter noise. (e) Approximated jitter noise. (f) Autocorrelation of jitter noise. (g) Power spectral density of jitter noise.

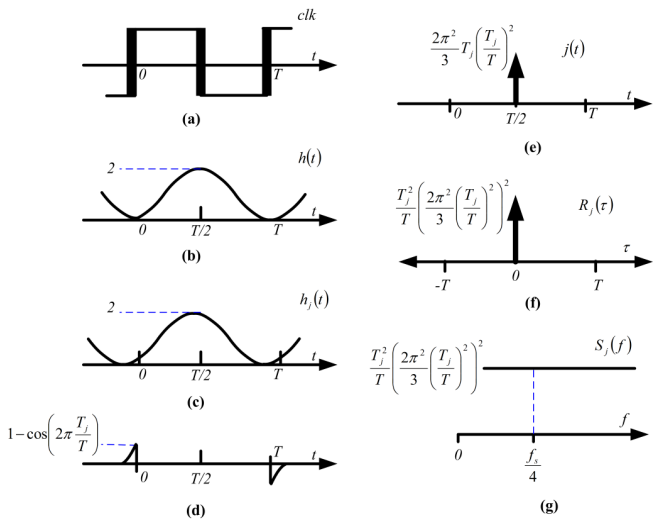

Fig. 3. Sine DAC jitter (a) Clock. (b) Ideal DAC pulse. (c) Jittered DAC pulse. (d) Jitter noise. (e) Approximated jitter noise. (f) Autocorrelation of jitter noise. (g) Power spectral density of jitter noise.

is much smaller than the clock period, it can be approximated as an impulse, as shown in Fig. 2(e):

$$j_{NRZ}(t) = 2\,T_j\,\delta(t) \tag{5}$$

where T_j is the rms clock jitter. Applying (2) and (3) to the NRZ jitter noise, and dividing by 2 to account for the probability of occurrence of a transition, we get:

$$R_{j_{NRZ}}(\tau) = \frac{2\,T_j^2}{T}\,\delta(\tau) \tag{6}$$

and

$$S_{j_{NRZ}}(f) = \frac{2\,T_j^2}{T} \tag{7}$$

The autocorrelation and the power spectral density of NRZ DAC jitter noise are shown in Fig. 2(f, g), respectively. The power spectral density is white and proportional to the clock jitter variance (T_j^2), which is consistent with the results obtained in [3], [4]. The jitter performance of NRZ DAC will be taken as the reference for other DAC types discussed in the next sections.

III. Sine DAC

Sine DAC (or raised-cosine DAC) shown in Fig. 3 was used by [1], [6] to reduce the sensitivity to clock jitter. The reason for jitter immunity of Sine DAC is the zero value and the zero slope of the output pulse at clock transitions [6]. The jitter noise of Sine DAC is calculated using (1) as shown in Fig. 3(b, c, d). The area of the jitter noise pulse can be calculated approximately using the first order Taylor expansion. Then, as done with NRZ DAC, the jitter noise of Sine DAC can be approximated as an impulse whose weight is equal to the area of the jitter noise pulse as shown in Fig. 3(e):

$$j_{sine}(t) = \frac{2\pi^2}{3} T_j \left(\frac{T_j}{T}\right)^2 \delta(t) \tag{8}$$

Applying (2) and (3) to Sine DAC jitter noise, we get:

$$R_{j_{sine}}(\tau) = \frac{T_j^2}{T}\left(\frac{2\pi^2}{3}\left(\frac{T_j}{T}\right)^2\right)^2 \delta(\tau) \tag{9}$$

and

$$S_{j_{sine}}(f) = \frac{T_j^2}{T}\left(\frac{2\pi^2}{3}\left(\frac{T_j}{T}\right)^2\right)^2 \tag{10}$$

The autocorrelation and the power spectral density are shown in Fig. 3(f, g), respectively. The jitter noise spectrum is white as in NRZ DAC, but with a significant noise reduction. The white spectrum indicates that the performance improvement is possible at any center frequency, which means that Sine DAC is effective for both lowpass and bandpass CT ΣΔMs.

IV. SC DAC

The authors of [4] studied the jitter effect in lowpass CT ΣΔMs, and differentiated between two types of jitter: width jitter, which is defined as the deviation of the DAC pulse width, and delay jitter, which is defined as the deviation of the DAC pulse position. It was concluded by the authors of [4] that the width jitter is the dominant source of SNR degradation, while the delay jitter can be ignored. Based on this assumption, SC DAC was used by [7], [8] to reduce the CT ΣΔMs sensitivity to clock jitter, because the width jitter is significantly reduced in SC DAC, due its exponential decay waveform.

All published results assured that the width jitter is the main source of SNR degradation, and that SC DAC is effective in reducing the modulator sensitivity to clock jitter. However, these results and conclusion are limited to lowpass CT ΣΔMs and can not be extended to bandpass CT ΣΔMs. The analysis presented in this section aims to quantify the jitter performance of SC DAC for both bandpass and lowpass CT ΣΔMs.

The SC DAC pulse is generated by charging and discharging a capacitor. Before the rising-edge of the clock, the capacitor is pre-charged to a certain value. At the rising-edge of the clock, the capacitor is allowed to discharge, and at the falling-edge of the clock, the capacitor is disconnected and the output current drops to zero as shown in Fig. 4(a, b). Unlike the NRZ DAC and Sine DAC, SC DAC is affected by both the rising-edge and the falling-edges of the clock. For this reason, the jitter analysis of SC DAC has to be split into two parts: the jitter effect due to the clock rising-edge, and the jitter effect due to the clock falling-edge. We will start with the falling-edge, because of its simplicity and apparent consistency with the published SC DAC jitter analysis in [7], [8].

A. SC DAC falling-edge jitter

The time-deviation of the falling-edge of the clock changes the width of the DAC pulse, but the difference in area between the jittered pulse and the ideal pulse is relatively small due to the decaying nature of the SC DAC pulse, as shown in Fig. 4(a-d). As the width of the jitter noise pulse is small compared to the clock period, it can be approximated as an impulse whose weight is equal to the area of the jitter noise pulse as shown in Fig. 4(e):

$$j_{SC_{falling}}(t) = T_j \frac{T}{RC} e^{-\frac{T}{2RC}} \delta(t - \frac{T}{2}) \tag{11}$$

Applying (2) and (3) to SC DAC falling-edge jitter noise, we get:

$$R_{j_{SC_{falling}}}(\tau) = \frac{T_j^2}{T} \left(\frac{T}{RC}\right)^2 e^{-\frac{T}{RC}} \delta(\tau) \tag{12}$$

and

$$S_{j_{SC_{falling}}}(f) = \frac{T_j^2}{T} \left(\frac{T}{RC}\right)^2 e^{-\frac{T}{RC}} \tag{13}$$

where RC is the exponential time constant. The autocorrelation and the power spectral density are shown in Fig. 4(f, g), respectively. The noise spectrum is white with a reduction in noise than NRZ case. SC DAC falling-edge jitter noise can be further decreased by decreasing RC, but this will increase the speed and the maximum current requirements of SC DAC [8].

B. SC DAC rising-edge jitter

The time-deviation of the rising-edge of the clock changes the position more than the width of the DAC pulse. The difference between the jittered pulse and the ideal pulse results in two opposite sign parts as shown in 5(a-d). The first part is a thin pulse similar to the one obtained in NRZ DAC case, and the second part is a decaying exponential. By approximating the thin pulse to an impulse, and assuming that the decaying exponential extends from zero to infinity, as shown in Fig. 5(e), we can simplify the jitter noise to:

$$j_{SC_{rising}}(t) = T_j \frac{T}{RC} \left(\delta(t) - \frac{1}{RC} e^{-\frac{t}{RC}}\right) \tag{14}$$

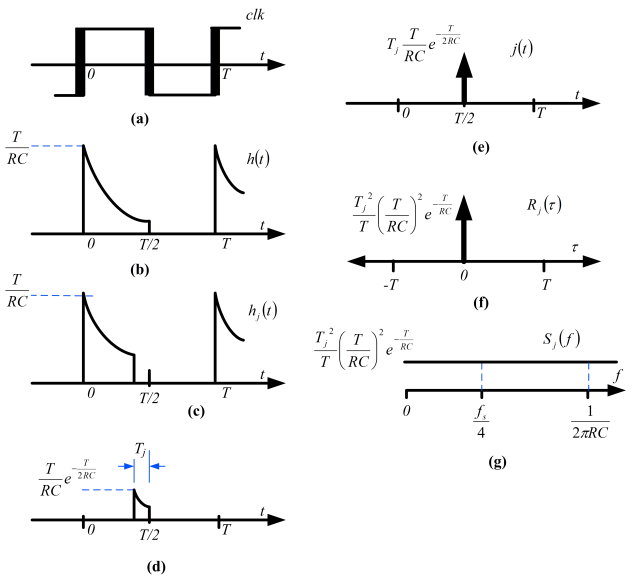

Fig. 4. SC DAC falling-edge jitter (a) Clock. (b) Ideal DAC pulse. (c) Jittered DAC pulse. (d) Jitter noise. (e) Approximated jitter noise. (f) Autocorrelation of jitter noise. (g) Power spectral density of jitter noise.

which is very similar to the impulse response of first order high-pass filter. Applying (2) and (3) to SC DAC rising-edge jitter noise, we get:

$$R_{j_{SC_{rising}}}(\tau) = \frac{T_j^2}{T} \left(\frac{T}{RC}\right)^2 \left(\delta(\tau) - \frac{1}{RC} e^{-\frac{\tau}{2RC}}\right) \tag{15}$$

and

$$S_{j_{SC_{rising}}}(f) = \frac{T_j^2}{T} \left(\frac{T}{RC}\right)^2 \frac{(2\pi fRC)^2}{1 + (2\pi fRC)^2} \tag{16}$$

The autocorrelation and the power spectral density are shown in Fig. 5(f, g), respectively. The noise spectrum is high-pass shaped, which indicates that the rising-edge jitter is small at low frequencies, but may be the dominant in high frequencies. This result is consistent with [4] and means that the delay jitter has a minor effect on lowpass CT ΣΔMs, but for bandpass CT-ΣΔMs which are usually centered at quarter the sampling frequency $(fs/4)$, delay jitter is the dominant. This makes SC DAC not suitable for bandpass CT ΣΔMs.

The total jitter noise of SC DAC can be obtained by summing the falling-edge jitter in (13), and the rising-edge jitter in (16):

$$S_{j_{SC}}(f) = \frac{T_j^2}{T} \left(\frac{T}{RC}\right)^2 \left[2\, e^{-\frac{T}{RC}} + \frac{(2\pi fRC)^2}{1 + (2\pi fRC)^2}\right] \tag{17}$$

The falling-edge jitter noise was multiplied by 2, to account for the width jitter that exist but ignored in the rising-edge jitter noise. For low frequencies, as in lowpass CT ΣΔMs, falling-edge jitter, i.e. width jitter, is the dominant and SC DAC jitter performance is better than NRZ DAC by about 5dB when using $RC = T/4$. For high frequencies, as in bandpass CT ΣΔMs centered at $f_s/4$, rising-edge jitter, i.e. delay jitter, is

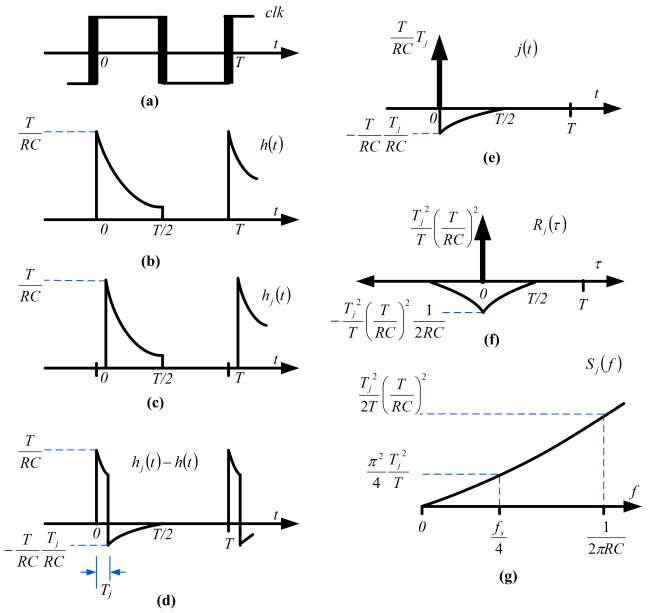

Fig. 5. SC DAC rising jitter (a) Clock. (b) Ideal DAC pulse. (c) Jittered DAC pulse. (d) Jitter noise. (e) Approximated jitter noise. (f) Autocorrelation of jitter noise. (g) Power spectral density of jitter noise.

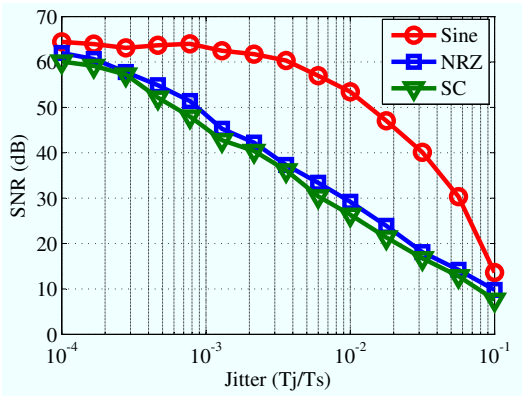

Fig. 6. Simulation Results

the dominant, and SC DAC jitter performance is worse than NRZ DAC by about 0.5 dB.

V. Simulation Results

To validate the jitter analysis done, a 4^{th} order bandpass CT $\Sigma\Delta$M centered at $f_s/4$ was designed with three different versions: with NRZ DAC, with Sine DAC and with SC DAC. The three modulators were simulated, and the clock jitter was swept from 0.01% to 10% of the clock period. For each value of the clock jitter, the maximum SNR of each modulator was measured and recorded. It can be concluded from the simulation results shown in Fig. 6, that SC DAC performance is slightly lower than NRZ DAC, while Sine DAC performance is significantly better than both, as was expected by the analysis.

VI. Conclusion

The jitter performance of CT $\Sigma\Delta$Ms for different DAC shapes was analyzed using a simple technique based on deriving the autocorrelation and the power spectral density of the jitter noise. An interesting conclusion is that in contrast to lowpass CT $\Sigma\Delta$Ms, bandpass CT $\Sigma\Delta$Ms have a worse jitter performance when using SC DAC instead of NRZ DAC. For both lowpass and bandpass CT $\Sigma\Delta$Ms, using Sine DAC seems to be the best solution regarding the jitter performance.

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