# A SWITCHED-CURRENT CLASS AB ΣΔ-MODULATOR

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## ABSTRACT

A class AB memory cell for SI-applications is presented. Important advantages of the class AB memory cell as linearity, low-consumption and high dynamic range are discussed. A fast system-level table-based simulation is used to optimize the circuit design. Simulation results for a second order ΣΔ-modulator are presented to show the high performance of the cell.

## I. INTRODUCTION

The switched-currents technique is generally considered as an alternative technique to switched-capacitors with the advantage that this class of circuits can be integrated in a standard digital CMOS technology [1]. However, the normally used class A SI-circuits have not achieved the same performance as SC-circuits in terms of precision, dynamic range, and power consumption. The precision limitation of SI-circuits is essentially related to the charge injection effect and the inherent non-linear behaviour of SI-memory cell as a building block. In a CMOS technology, complementary devices allow the implementation of class AB circuits. Two well-known features of current-mode class AB circuits are their high dynamic range and low power consumption. Another important feature of these circuits is their linearization effect which will be discussed here. Most of the presented class AB current memories don't exploit all of the advantages of class AB operation [2,3,4]. However, a sigma-delta modulator based on the memory cell proposed in [5] has given interesting results [6]. The main disadvantage of this class AB memory cell is the high aspect ratio of the memory transistors. This reduces considerably the precision of the memory cell and consequently increases the loss of the integrator realized by this kind of memory cell.

Recently, a low input-resistance class AB current-conveyor has been presented in [7,8]. This CCII can be used with few modifications as a current memory-cell for SI-applications. In this paper, we discuss some features of this memory cell and its main design guidelines. Finally, the results of a table-based simulation for a classical second-order sigma-delta converter are presented.

## II. BASIC CLASS AB MEMORY CELL

The basic memory cell is shown in Fig.1. During the phase $\phi_2$, the input current is memorised by the two transistors MN and MP and during the phase $\phi_1$, the memorised current is delivered to the output. The transistors TN2 and TP2 realize a grounded-gate amplifier which maintain the voltage of the input node near to ground potential. This improves the memory cell precision in comparison with the circuit of [5] because the precision of a memory cell is mainly related to the memory transistor gate-source voltage. Since in this circuit the drain-source voltages of the memory transistors are relatively constant and about $V_{dd}/2$, their gate-source voltages can be larger with a higher swing $(\approx V_{dd}/2 - V_{TH} - V_{dsat})$ than in the cascoded version of the conventional circuit in [5]. This allows us to design the cell with a lower aspect ratio for the memory transistors. In the conventional circuit, transistors must have large aspect ratios in order to reach a modulation index of 4 while maintaining all of the transistors in saturation. Another advantage of the presented circuit is its simpler switch connections.

The linear input characteristics of the current-mode class AB circuits have already been discussed in [7,8]. Here, we discuss other linearization effects which are especially important in SI-circuits. First, we mention that although the current handled by a class AB memory cell can be much larger than its quiescent current $I_0$, we limit the input current to $\pm 4I_0$. In this region the circuit has a linear behavior and consequently the errors produced by the circuit can be expected to be proportional to the input current.

It should be noted that because of using a floating voltage source, the bias current of this cell depends on the supply voltage. So, it is necessary to control the sources $I_{B2}$ in such a way that the bias current of the cell remains constant. In a complex circuit, as in a ΣΔ-modulator, only one controlling circuit may be sufficient to control all of the current sources $I_{B2}$.

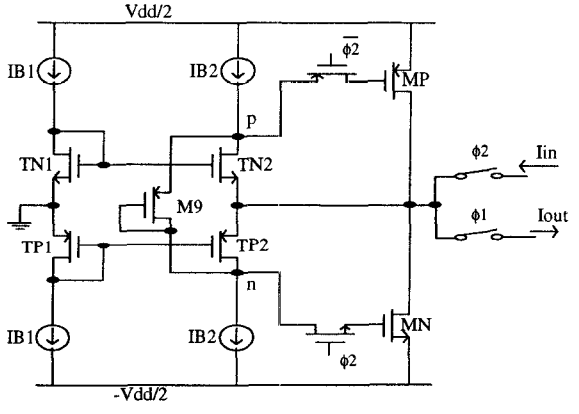


Fig.1, Basic class AB SI-memory cell.

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## III. NON-IDEAL BEHAVIOR

**Output to input conductance ratio error.** This error is decreased by increasing the input conductance of the cell using the grounded-gate amplifiers TN2 and TP2. The current sources $I_{B2}$ are cascoded because they are subject to the most important voltage variations in the circuit. Because the memory has a large current swing, the variation of the transistors output resistance as a function of the input current must be considered. Analytical calculations and simulations show that the error due to output conductance of the transistors is highly linear[9].

**Settling error.** Because of using a floating voltage source to obtain class AB operation, the settling time of the circuit has little variation with respect to the input current amplitude[7]. Uniform settling behavior has a great importance in sigma-delta modulators because it allows the increase of the sampling frequency without needing a precise settling[12].

**Charge injection error.** Detailed analysis, using first order models show that the injected current is highly linear [9]. A charge injection analysis of the memory cell was carried out for a 0.5μm CMOS technology using the charge injection model presented in [10,11]. The quiescent current of the memory was 25μA. The dimensions of the NMOS and PMOS memory transistors were, respectively, 26μ/10μ and 52μ/5μ and the clock signal had a fall time of 10nS. Fig.2 shows the injected current as a function of the input current. The two switch transistors have identical dimensions 0.8μ/0.5μ. It is observed that the current error in the region ±100μA is highly linear. The slope of the curve depends on the switches width. Fig.3 represents THD of the memory cell due to charge injection. The switches have equal lengths $L_n = L_p = 0.5\mu m$ with a width ratio, $WR = W_p/W_n$, varying between 1 and 4. The figure shows that harmonic distortion is a function of the relative value of the switches width. The switches width determines also the error value and the integrator loss. Therefore, the choice of the switches width is a trade-off between settling error, charge injection error value and THD.

**Dynamic range.** Three essential factors which determine the dynamic range of a memory cell are: memory capacitance, gate-source voltage of the memory transistor, bias current and modulation index. A memory capacitance of 1pF gives a good trade-off between speed and dynamic range. Class AB operation allows a modulation index of 4 in conjunction with a low bias current. In addition, the cell can be designed with a high gate-source voltage. Excluding the current sources noise, calculations give a dynamic range of about 76dB for a lossless integrator [9].

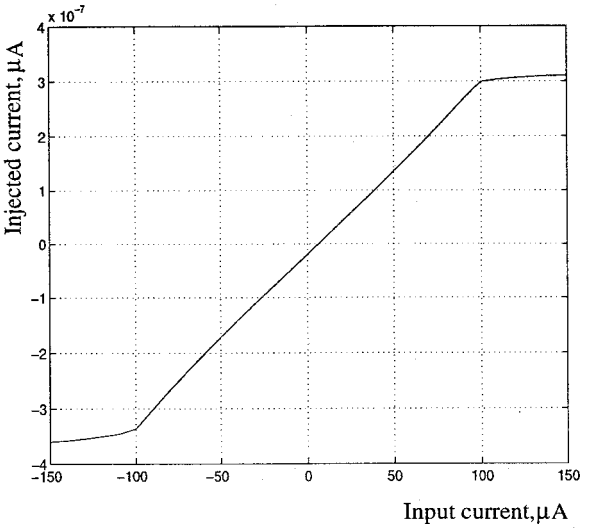



Fig.2, Current-injection error in the memory cell.

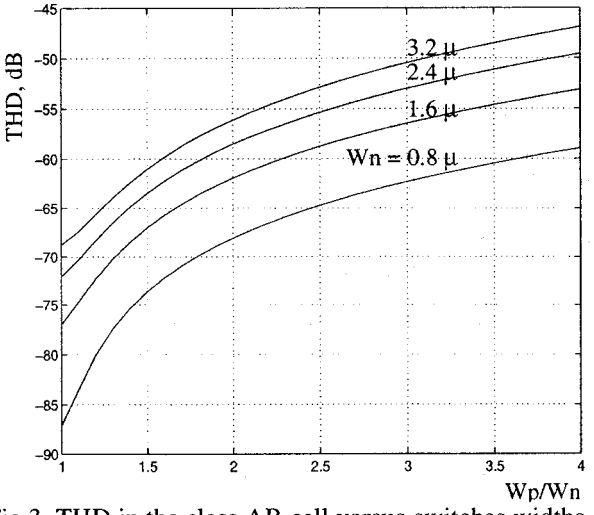



Fig.3, THD in the class AB cell versus switches widths.

## IV. TABLE-BASED SIMULATION OF A SECOND-ORDER Σ-Δ MODULATOR

The presented class AB memory cell was used to implement the second-order sigma-delta modulator of [12] in a 0.5μm CMOS technology. The supply voltage was 3.3V and the bias current of the cells 25μA. The circuit was clocked at a rate of $f_s = 10MHz$. A table-based simulation was used to take into account non-idealities of the memory cells. In the first step of the simulation process, a memory cell is simulated using the electrical simulator ELDO in order to generate three tables containing the errors due to charge injection, output conductance and settling. The step value is taken as 1μA. Sufficient care must be taken in the measurements so that each error is isolated from the others. The first and second tables are one dimensional because the corresponding errors depend only on the input current of the memory cell. The third table is two dimensional because the settling error depends both on the initial current of the memory cell and the input current.

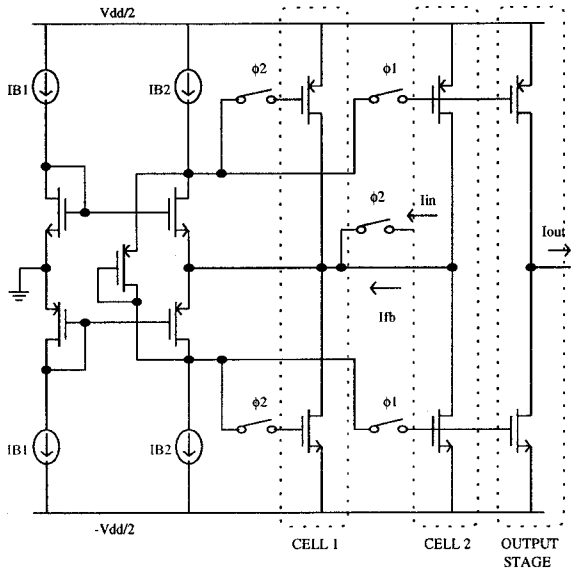



Fig. 4, Lossless class AB SI-integrator.

Polynomial fitting is used to replace the two first tables by two vectors containing the coefficients of the equivalent polynomials. In the same way, the third table is replaced by a matrix containing the coefficients of the polynomials. Replacing the tables by polynomials, reduces considerably the look-up time because each error is obtained by a direct substitution of the variables in the polynomial expressions. Hence, SI-integrators, Fig.4, can be replaced by the model of Fig.5 in order to introduce the errors. The model was developed in a SIMULINK-MATLAB environment to take advantage of its system implementation flexibility. Integrator output current is calculated using difference equations and by adding the errors generated by each internal memory cell. It should be noted that the internal current swing of a SI-integrator is smaller than its input signal swing. In fact, during phase $\phi_2$, the input current of the integrator is added to the current fedback from the second cell. So, if the currents have the same sign, the memorised current in the first cell will be larger than the input current of the integrator.

The spectral density of the modulator output affected by each source of error is shown in Fig.6. An ideal comparator was used and the input signal frequency was $f_{in} = (7/8192)f_s$. It is observed that the even harmonics are heavily attenuated due to circuit symmetry. Evaluating the impact of each source of error on the global system performance allows us to optimize the circuit design with respect to each error. The corresponding signal to (Quantization noise + Harmonic distortion) ratio for OSR=128 are illustrated in Fig.7. This ratio for the ideal system and the system containing the three errors is compared in Fig.8. A maximum SNDR of 85dB equivalent to 14bits is observed.

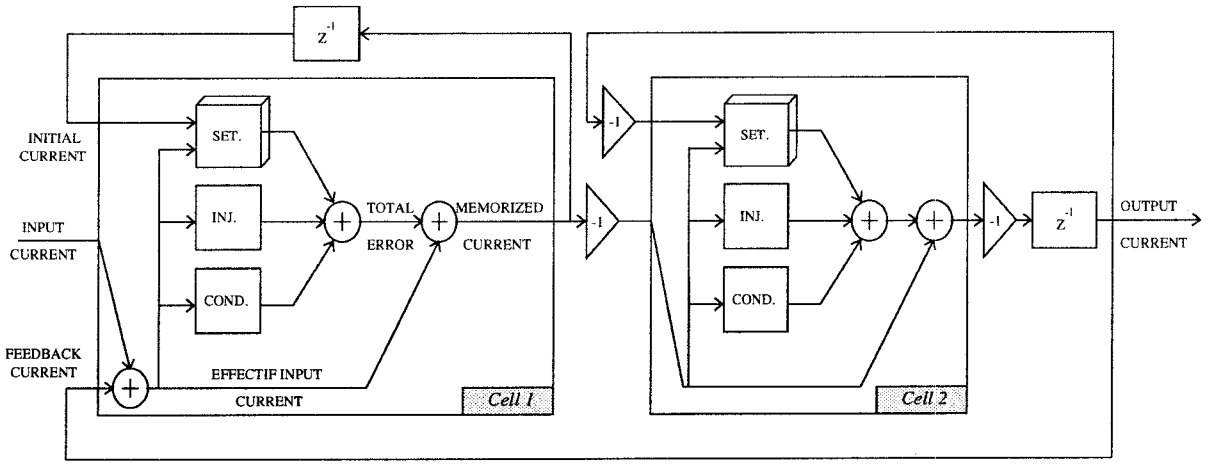
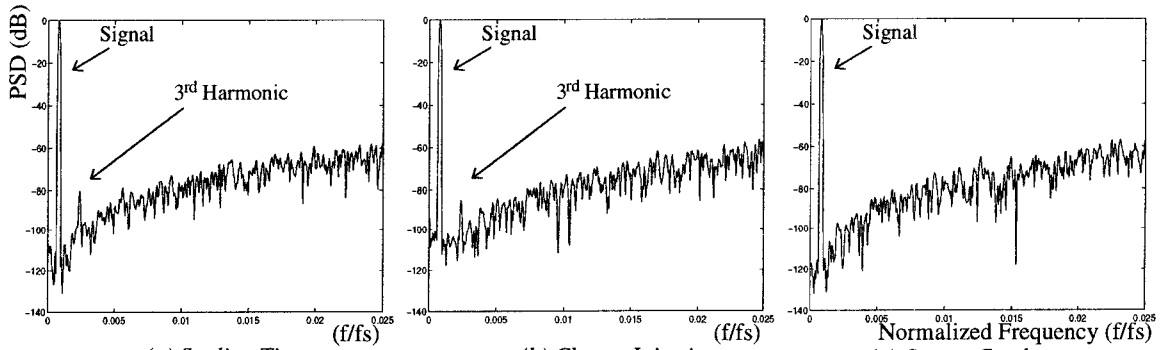



Fig.5, Integrator model taking into account the non-idealities.




*(a) Settling Time* *(b) Charge Injection* *(c) Output Conductance*

Fig.6, Modulator output spectral densities due to each source of error

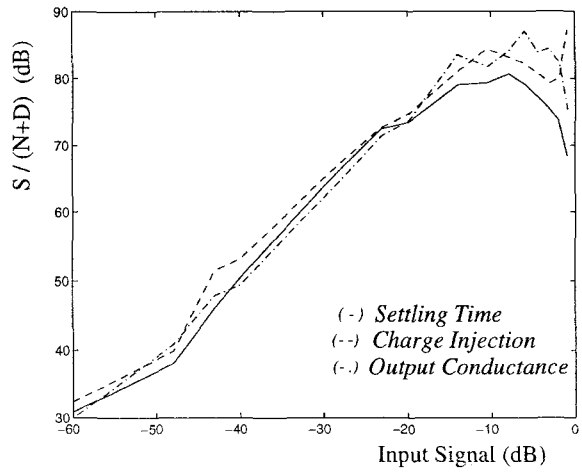



Fig.7, SNDR due to each non-ideality..

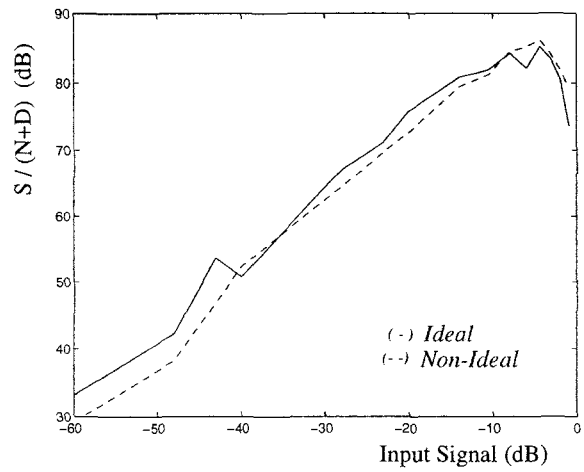



Fig.8, SNDR for the ideal and the SI-based systems.

Experimental results have not been ready in time for the paper but they will be presented during the conference.

## VI. CONCLUSION

A class AB current memory cell operating with a supply voltage of 3.3V was presented. The most interesting features of the class AB cell such as low power consumption, high linearity , uniform settling, and high dynamic range were discussed. A table-based simulation method, developed with the universal mathematical tool SIMULINK, allows us to predict the performance of the basic cell in system level. This particularity and the possibility of evaluating the impact of each non-ideality allow the optimization of the circuit with respect to each source of error. Other SI-based systems, such as filters, can also be simulated using the presented model. It should be noted however, that the glitches and mismatch effects are not taken into account.

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