A Clock-less 8-bit Folding A/D Converter

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***Abstract*—This paper presents a continuous-time 8-bit folding analog-to-digital converter. The clock-less architecture is composed of 8 identical stages with 1 bit/stage. The circuit is designed in a 350nm CMOS process with a supply voltage of 3.3V. Simulation results show that the 8-bit clock-less ADC can achieve a Signal-to-Noise and Distortion Ratio of 53dB. The ADC has a power consumption of 5.51mW. The proposed circuit is compared with a similar continuous-time 8-bit pipeline ADC with 1 bit/stage.**

Keywords: *Analog-to-Digital Converter, Continuous-Time, Clock-less, Asynchronous, CMOS.*

I. INTRODUCTION

Clocked processors have dominated the computer industry since the 1960s because chip designers saw them as more reliable, capable of higher performance, and easier to design and test than their clock-less counterparts. The clock establishes a rhythm that drives all chip, and this time constraints make design easier by reducing the n5umber of control decisions [1].

In synchronous designs, the data moves on every clock edge, causing voltage spikes. In clock-less chips, data are not all produced at the same time, which spreads out current flow, thereby minimizing the strength and frequency of spikes and emitting less electromagnetic interference (EMI). Less EMI reduces both noise-related errors within circuits and interference with nearby devices [1].

Asynchronous chips have no clock and each circuit powers up only when used, so asynchronous processors use less energy than synchronous counterparts [1].

Moreover, regular sampling time uncertainty introduces additional errors when analog signals are sampled at equal time intervals and reconstructed at time intervals that show a timing uncertainty or vice versa. Sampling clocks show short term and long term time jitter. Especially the short term time jitter has influence on the performance of a converter [2].

In continuous-time system the amplitude can be quantized into discrete amplitude levels, resulting in an amplitude discrete signal. This operation can be performed to maintain well-defined amplitude levels when signals pass through several processing stages.

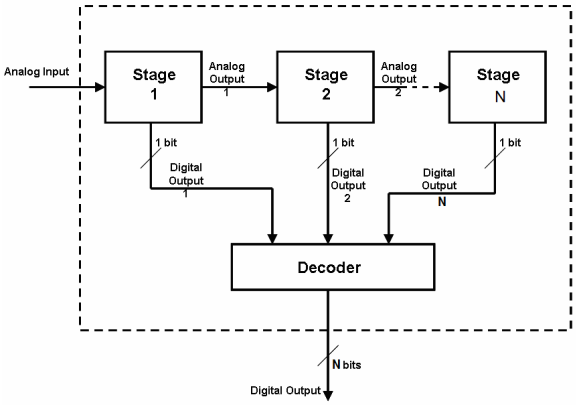

Figure 1. Block diagram of the clock-less folding ADC with 1-bit/stage.

Reference [3] has confirmed that continuous-time signal processing is possible, and that it presents several advantages in comparison to the classical discrete-time case: no signal aliasing, no quantization error aliasing, this avoids sub-harmonic components, and reduces the in-band quantization error power.

Analog-to-digital converters (ADCs) are usually specified to have a fixed conversion time, but clock-less ADCs is gaining relevance in many fields, ranging from astronomy to medicine [4]. Some applications in equipments of the medical area, such as X-rays and spectrometry equipments need ADCs that are activated by the beginning of the event and closed down in the end, to control the energy sent during the event. Thus, the conversion time has a large range of variations [5]. In this paper we propose an architecture for a clock-less 8-bit 1-bit/stage folding ADC. The architecture is compared with a clock-less 8-bit 1-bit/stage pipeline ADC.

II. BASIC CONCEPT OF THE CONVERSION TECHNIQUE

The general architecture of the proposed clock-less ADC is shown in Fig. 1. This structure is a folding architecture. It is one of a number of possible serial or bit-per-stage architectures. It consists of a cascade of identical stages, with one 1-bit sub-ADC and a gain stage multiplying by either 2 or -2.

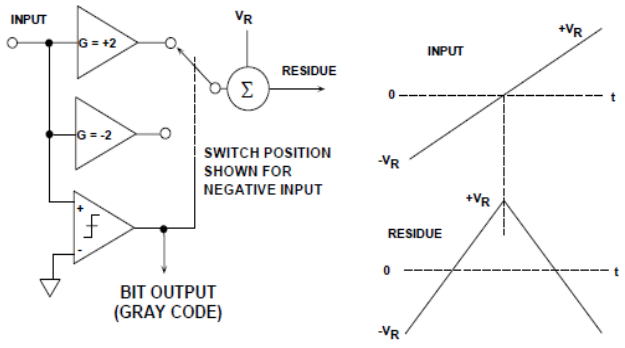

Figure 2. Conversion algorithm of a folding ADC stage [9].

The idea behind this A/D converter is based on the general rectification algorithm [6]:

$$V_{out} = 2 \mid V_{in} \mid - V_{Ref} \qquad (1)$$

A block diagram of one stage of this ADC along with its input and output signal waveforms are shown in Fig.2. Single-ended current-mode implementations have been proposed in [6,7,8].
In this work, we propose to build the conversion algorithm illustrated in Fig.2, using the differential voltage-mode circuit shown in Fig.3. The output voltage of each stage of the proposed clock-less ADC is as follows:

$$V_{outp} = V_{DP} (2*V_{inn} + V_{refp}) + V_{DN} (2*V_{inp} + V_{refp}) \qquad (2)$$

$$V_{outn} = V_{DP} (2*V_{inp} + V_{refn}) + V_{DN} (2*V_{inn} + V_{refn}) \qquad (3)$$

The conversion algorithm of the folding ADC stage, shown in Fig.2, is similar to the conversion algorithm of the pipeline ADC, shown in Fig.4. Similarly, the differential architecture of a clock-less folding ADC, Fig.3, is similar to the differential architecture of a differential clock-less pipeline ADC, Fig.5.
One problem of clock-less pipeline ADCs is the strong discontinuity in the residue output waveform. In clock-less ADCs a sample is captured only when the analog input signal crosses a reference level. In this moment, a voltage value is added or subtracted from the value of the analog input signal. This results in stringent requirements for the operational amplifier to maintain a well-defined amplitude levels when signals pass through several processing stages.

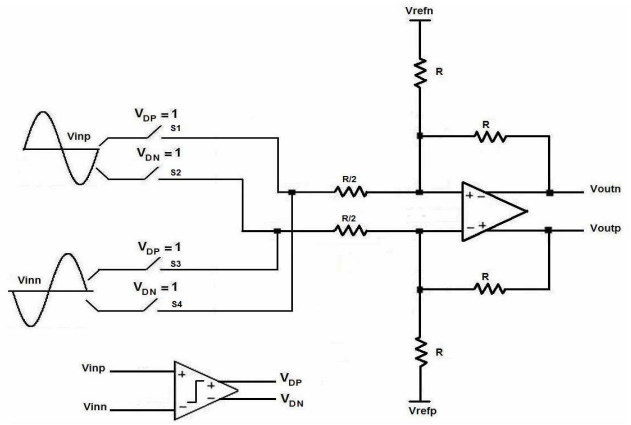

Figure 3. Differential realization of one stage a clock-less folding ADC.

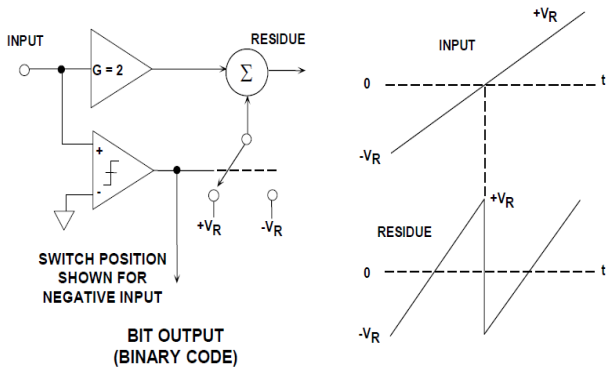

Figure 4. Conversion algorithm of a pipeline ADC stage [9].

In the proposed clock-less ADC, when the analog input signal crosses the reference levels, only the sign of the signal is inverted, thus relaxing the requirements on the operational amplifier. This scheme has often been referred to as serial-Gray (since the output coding is in Gray code), or folding converter because the shape of the transfer function. Performing the conversion using a transfer function that produces an initial Gray code output has the advantage of minimizing discontinuities in the residue output waveforms and offers the potential of operating at higher speeds than the more conventional binary approach [10].

Fig. 6 shows the input analog signal, the output analog signal and the output digital signal of the first block of the proposed clock-less folding ADC. This figure shows that in each point of comparison between the input analog signal and Vref, a transition is generated in the output digital signal.
Fig. 7 shows the input analog signal, the output analog signal and the output digital signal of the first block of the pipeline ADC.

III. CIRCUIT DESIGN

The first step in designing the proposed clock-less folding ADC is to determine the operational amplifier specifications. A complete model of an 8-bit clock-less folding ADC, using the 1-bit architecture illustrated in Fig.3, was build using macro-models for the differential operational amplifiers. This model was used to determine the minimum specifications of the operational amplifier specifications in order to achieve a Signal-to-Noise and Distortion Ratio (SNDR) higher than 50dB

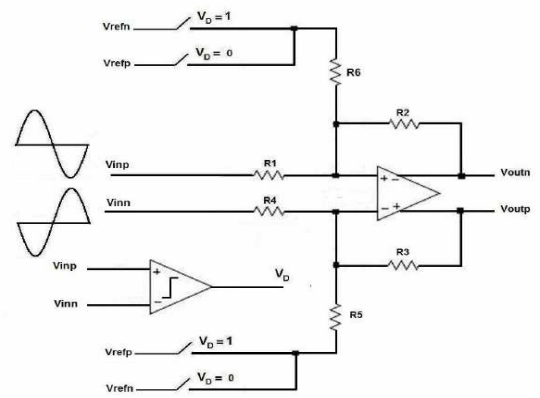

Figure 5. Differential realization of one stage a clock-less pipeline ADC.

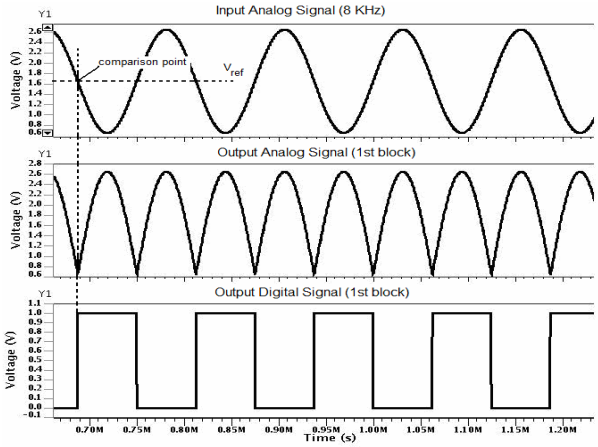

Figure 6. Clockless folding ADC: 1.Input Analog Signal (Vinp). 2. Output Analog Signal (Voutp - 1st stage). Output digital signal (V_{DP} - 1st stage).

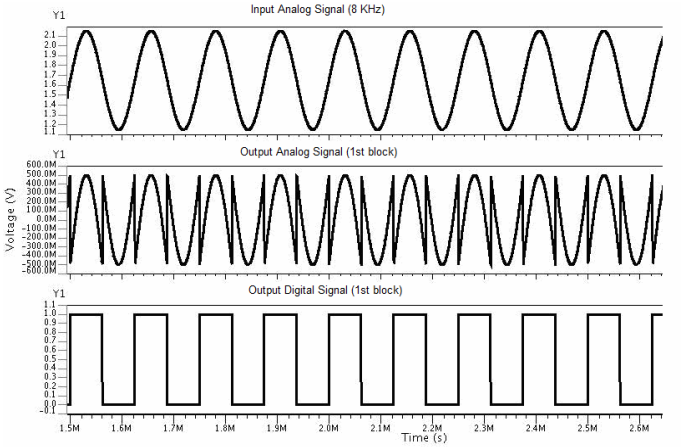

Figure 7. Clockless pipeline ADC: 1.Input Analog Signal (Vinp); 2. Output Analog Signal (Voutp - 1st stage); 3. Output digital signal (V_{DP} - 1st stage).

In order to calculate the SNDR, first the digital output is passed through an ideal DAC, second the continuous-time analog output is sampled using a high sampling rate compared to the input signal frequency range and finally an FFT is performed on the sampled signal. An SNDR higher than 50dB was achieved with a DC-Gain of 70dB and a Gain-Bandwidth-Product of 45MHz.

Note that a conventional 8-bit discrete-time ADC cannot theoretically achieve a SNR higher than 49.76dB (6N+1.76dB). These results support claims made in [3] that continuous-time ADCs have lower quantization noise than their discrete-time counterparts.

The operational amplifier used in the design of the 1-bit/stage ADC is show in Fig. 8. This is a two-stage amplifier using Miller technique for frequency compensation. The use of differential operational amplifiers brings several advantages as high rejection of supply noise and higher output swings.

This differential amplifier was designed in 350nm CMOS technology for the specifications determined in the previous section. The transistor sizes of the operational amplifier are shown in table I and the simulated amplifiers specifications are show in table II.

IV. Simulation Results

The operational amplifier used in the design of the 1 bit/stage ADC is show in Fig. 8. This is a two-stage amplifier using Miller technique for frequency compensation. The use of differential operational amplifiers brings several advantages as high rejection of supply noise and higher output swings.

The transistor sizes of the operational amplifier are shown in table I and the amplifiers specifications are show in table II. This amplifier is used to design an 8-bit clock-less folding ADC based on the architecture illustrated in Fig.3 and an 8-bit clock-less pipeline ADC based on the architecture illustrated in Fig.5.

Both ADCs are simulated by applying a sinusoidal signal with maximum signal amplitude and a frequency of 8 kHz. Fig.9 shows the FFT of the output of the clock-less folding ADC. It can be seen that the 3rd harmonic is around -60dB and that the folding ADC achieves a maximum SNDR of 53 dB in a 50 kHz bandwidth.

Fig.10 shows the FFT of the output of the clock-less pipeline ADC. Notice the presence of harmonics and sub-harmonics having amplitudes higher than -50dB. The maximum SNDR achieved by the clock-less pipeline ADC is 42dB.

The performance and the circuit characteristics of both ADCs are listed in table III. From this table, we can see that if the same operational amplifier is used, a clock-less folding ADC achieves higher performance than a clock-less pipeline ADC.

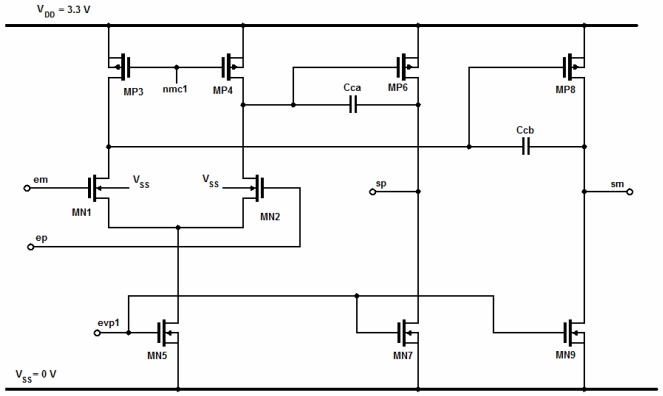

Figure 8. Two-stage differential amplifier.

TABLE I. Dimensions of the operational amplifier's transistors.

Transistors	W/L (µm/µm)
MN1, MN2	2.2/0.7
MP3, MP4, MP6, MP8	7.25/0.7
MN5. MN7, MN9	4.85/0.7

TABLE II. Specifications of the operational amplifier

Ao	71.65 dB
F_T	45.4 MHz
SR	23.5 V/µs
Consumption	140 µW

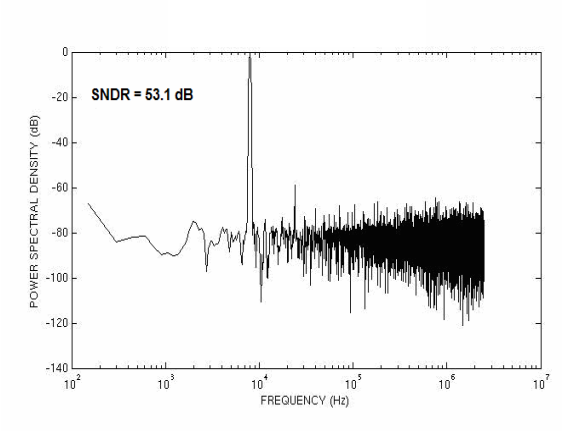

Figure 9. The Power Spectral Density of the output of a clockless Folding ADC using the two-stage differential amplifier of Fig.8 and the dimensions of Table I.

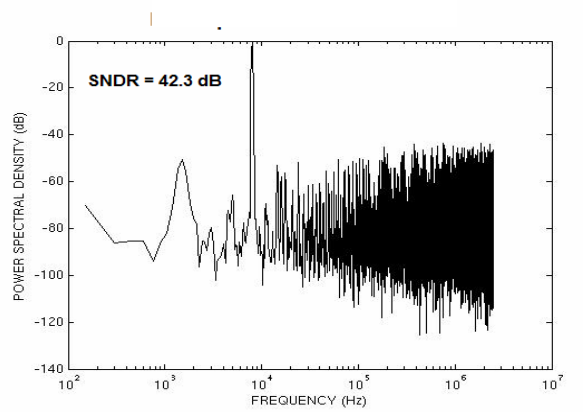

Figure 10. The Power Spectral Density of the output of a clockless Pipeline ADC using the two-stage differential amplifier of Fig.8 and the dimensions of Table I.

TABLE III. COMPARISON FOLDING – PIPELINE

	Folding	Pipeline
Input Frequency (fin)	8 KHz	8 KHz
DC Gain (amp.)	75.51 dB	75.51 dB
GBW (amp.)	45.4 MHz	45.4 MHz
Resolution	8 bits	8 bits
Power consumption (Analog Parts)	5.51 mW	6.28 mW
ENOB	8.53 bits	6.88 bits
SNDR	53.1 dB	43.2 dB

V. CONCLUSIONS

In this paper, we propose an architecture for a clock-less folding ADC. The proposed 1-bit stage is based on a differential voltage-mode circuit. A similar architecture is also proposed for a differential clock-less Pipeline ADC.

The required operational amplifier specifications were determined by simulation in order to obtain the desired clock-less Folding ADC performance. The op-amp was designed and integrated in the complete model of a clock-less 8-bit Folding ADC and a clock-less 8-bit Pipeline ADC. Simulation results have shown that the clock-less folding ADC achieves a better performance than his Pipeline counterpart.

VI. ACKNOWLEDGEMENTS

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