Automatic Design of RF Linear Transconductor

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***Abstract*—This work proposes a methodology to design linear transconductors based on three circuit topologies previously reported in literature. The design is done to be used in a synthesis tool, containing the MOS transistor model. The topologies has been analyzed using a more improved small-signal equivalent circuit of a MOS transistor to obtain a more accurate expression for the transconductance (Gm) and to extend the use for high frequencies range. A design examples in $945Mhz$ is given in a $130nm$ CMOS process.**

I. Introduction

The transconductor is a basic build block in analog and RF circuits applications and the quality of the transconductors determines the performance of circuits. One of the most important specifications of a transconductor is its linearity [1] because this can determine the overall linearity of the system. In filters designs, for example, the transconductors are the critical part since they may limit the linearity and the noise performances [2]. For this reason for many years several ways to increase the linearity of the MOS transconductance have been investigated [3]–[6].

In this work, we propose an automatic design method that provides the desired transconductance and does not require any iterations with a circuit simulator. In this method all transistors and resistors, are calculated using the complete small-signal model for transistors.

In section II, three transconductance linearization techniques used in this work are reviewed. A circuit analysis is carried on to obtain an accurate symbolic expression for (G_m). For techniques based on resistor degeneration an expression for the degeneration resistor(R) is derived. In section III, it is shown how a synthesis tool can be used to design linear transconductance circuits, using the new expressions for Gm and R. Finally design examples and simulation results are presented in section IV.

II. Topologies for Linear MOS Transconductors

In this section, three techniques to linearize the MOS transconductor are analyzed. The first and second ones are the MOS differential pair with resistive source degeneration with two different implementations. The third one is the MOS transistor degeneration obtained by two transistors operating in ohmic region [2], replacing the resistors in the first case.

A. Resistive Source Degeneration

Better linearity can be archived for large effective gate-to-source voltages, however, this is particularly critical for low-voltage applications.

On the other hand, one simple way to linearize the transconductor is source degeneration using resistors, as represented in Fig.1(a)-1(b), where both topologies realize the same transconductance, with different properties. In Fig.1(a) the noise of the sink appears at the output as common noise, but the resistor causes a voltage drop and reduces the common mode swing of the input signals. For the Fig.1(b), the noise of each sink appears as differential noise in output [4]. The disadvantage of these configuration are the large value resistors needed to archive a wide linear input range [2].

To analyze the circuits of Fig.1(a)-1(b), the half-circuit concept simplified model is employed, since the circuit is symmetrical and the input is differential. The Fig.2 shows the equivalent half-circuit of the circuit of Fig.1(a).

Essential frequency-dependent behaviors can be investigated using a more sophisticated small-signal transistor model. Therefore, the RF transistor model was employed here [7], [8], with a small modification: the gate, drain and source resistances were ignored, because they are not yet implemented in synthesis tool utilized to validate this approach.

Using the circuit of the Fig.2 to obtain the transconductance gives:

$$z_1 = \frac{1}{j\omega C_{gd}} \tag{1}$$

$$z_2 = \frac{1}{j\omega(C_{gs} + C_{gb})} \tag{2}$$

$$z_3 = \frac{1}{gds_1 + j\omega(C_{sd} + C_{bd})} \tag{3}$$

Defining $G_m = i_{out}/v_{in}$, we can found

$$Gm_{d1} = -\frac{z_{a_3}R + z_{a_4} - z_{a_1} - z_1 z_2}{(z_{a_3} z_{load} + z_{a_2} + z_{a_1})R + z_{a_4} z_{load} + z_2 z_{a_2} - z_1 {z_2}^2} \tag{4}$$

where Z_{load} is the load resistance.

Similarly for the circuit of Fig.3, equation (10) can be found, where

$$z_4 = \frac{1}{gds_2 + j\omega(C_{sd_2} + C_{gd_2} + C_{bd_2})} \tag{5}$$

$$z_{a_1} = (gmz_1 z_2 z_3) \tag{6}$$

$$z_{a_2} = (z_1(z_3 + z_2)) \tag{7}$$

$$z_{a_3} = (gmz_2 + 1)z_3 + z_2 + z_1 \tag{8}$$

$$z_{a_4} = (z_2(z_3 + z_1)) \tag{9}$$

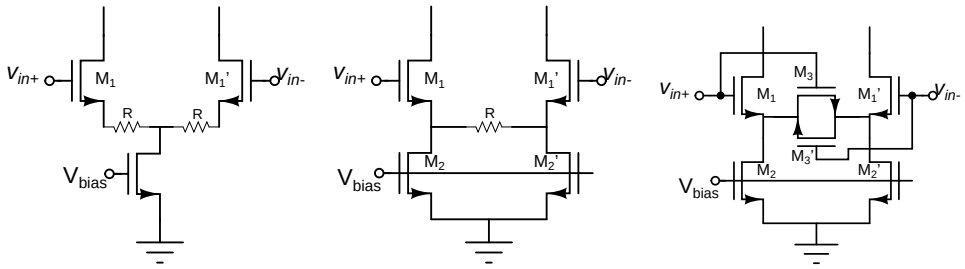

Fig. 1. Transconductance Topologies

$$Gm_{d2} = -\frac{(z_{a_4} + z_4 z_{a_3} - z_{a_1} - z_1 z_2)R + 2z_4 z_{a_4} - 2z_4 z_{a_1} - 2z_1 z_2 z_4}{((z_{a_4} + z_4 z_{a_3})z_{load} + (z_4 + z_2)z_{a_2} + z_4 z_{a_1} - z_1 z_2{}^2)R + 2z_4 z_{a_4} z_{load} + 2z_2 z_4 z_{a_2} - 2z_1 z_2{}^2 z_4} \tag{10}$$

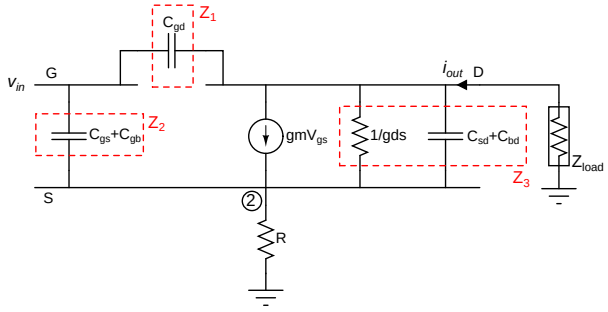

Fig. 2. Small-Signal model for Transconductance (a) and the Output resistance(b)

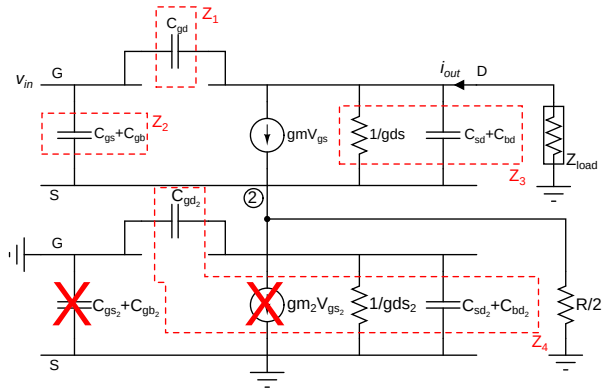

Fig. 3. Half-Circuit Small-Signal Model

B. MOS Transistors Source Degeneration

Fig.1(c) shows a solution proposed in [3] using a four-transistor input stage, for which the transconductance is linearized by the voltage-controlled degenerating resistors, realized with MOS transistors in the ohmic region. Considering perfectly matched transistors $M_1 - M_1^{'}$, $M_3 - M_3^{'}$, neglecting the channel length modulation and considering that all transistors has its bulk connected to its source, the transfer characteristic of this transconductor is given by [3]

$$G_m = \left.\frac{\partial I_{out}}{\partial v_{in}}\right|_{v_{in}=0} = \frac{I_{bias}}{a(V_{gs} - V_{th})_{M_1}} \tag{11}$$

where

$$a = 1 + \frac{\beta_1}{4\beta_3} \tag{12}$$

and

$$\beta = \mu C_{ox}\frac{W}{L}. \tag{13}$$

The authors in [2], [3] show that one can increase the input linear dynamic range adjusting the parameter a and the optimum value of the ratio for the best linearity performance was found near to 2.75 [3]. But, the equation (11) is not sufficiently accurate to be implemented, (as for example, for a given circuit with a desired transconductance around $1mS$, the value obtained was $Gm = 800\mu S$). So analyzing the circuit of Fig.4, which is similar to the resistors degenerated topologies, we can find equation (23), where

$$z_5 = \frac{1}{j\omega(C_{gd_3})} \tag{14}$$

$$z_6 = \frac{1}{2(gds_3 + j\omega(C_{sd_3} + C_{bd_3}))} \tag{15}$$

$$z_7 = \frac{1}{j\omega(C_{gs} + C_{gb} + C_{gs_3} + C_{gb_3})} \tag{16}$$

$$z_{a_5} = ((gmz_4 + 1)z_5 + z_4)z_6 + 2z_4 z_5 \tag{17}$$

$$z_{a_6} = (1 - gmz_1)z_4 \tag{18}$$

$$z_{a_7} = (z_3 + z_1)z_4 z_5 z_6 \tag{19}$$

$$z_{a_8} = (z_4 + z_3)z_5 + z_3 z_4 \tag{20}$$

$$z_{a_9} = z_5 z_6 z_7 \tag{21}$$

$$z_{a_{10}} = z_1 z_3{}^2(z_5 + z_4)z_6 \tag{22}$$

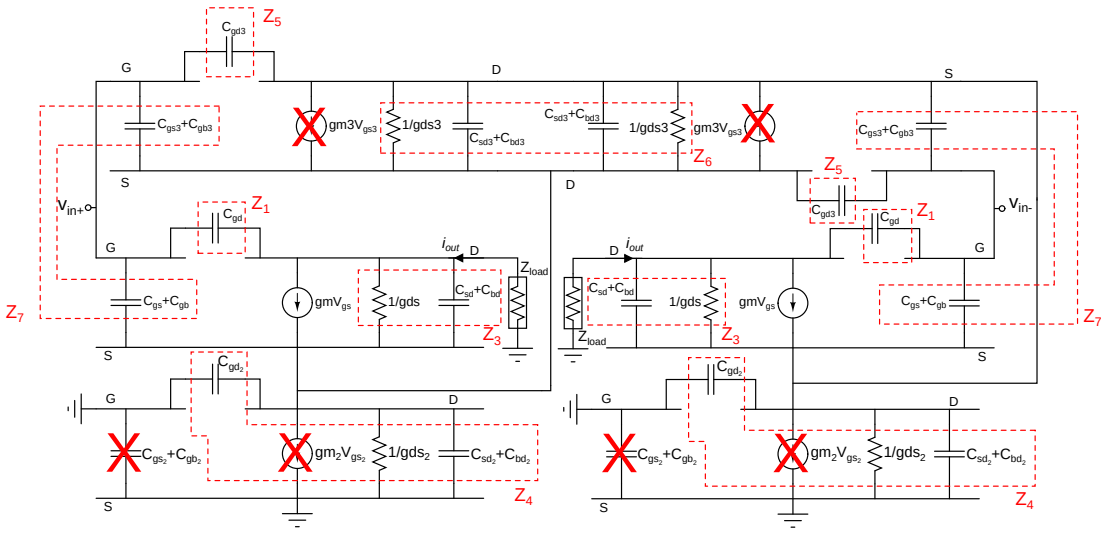

Fig. 4. MOS Degenerated Small-Signal

$$Gm_{d3} = -\frac{(z_{a_6} - z_1)z_{a_9} + z_{a_7} + z_{a_4}z_{a_5} + ((-z_5 - 2z_4)z_6 - 2z_4z_5)z_{a_1} + (-2z_1z_4z_6 - 2z_1z_4z_5)z_7}{(z_{a_6}z_{a_9} + z_{a_7} + z_{a_4}z_{a_5})z_{load} + z_6z_{a_2}z_{a_8} + 2z_3z_4z_5z_{a_2} - z_{a_{10}} + z_4z_5z_6z_{a_1} - 2z_1{z_3}^2z_4z_5} \quad (23)$$

$$R_{d1} = -\frac{Gmz_{a_4}z_{load} + z_{a_4} + Gmz_2z_{a_2} - z_{a_1} - Gmz_1{z_2}^2 - z_1z_2}{Gmz_{a_3}z_{load} + z_{a_3} + Gmz_{a_2} + Gmz_{a_1}} \quad (24)$$

$$R_{d2} = -\frac{2Gmz_4z_{a_4}z_{load} + 2z_4z_{a_4} + 2Gmz_2z_4z_{a_2} - 2z_4z_{a_1} + (-2Gmz_1{z_2}^2 - 2z_1z_2)z_4}{(Gmz_{a_4} + Gmz_4z_{a_3})z_{load} + z_{a_4} + z_4z_{a_3} + (Gmz_4 + Gmz_2)z_{a_2} + (Gmz_4 - 1)z_{a_1} - Gmz_1{z_2}^2 - z_1z_2} \quad (25)$$

III. Design Methodology

A. CAIRO+

The synthesis tool used in this work is the CAIRO+, a framework developed at the LIP6 laboratory to help analog designers with their projects, with the advantages of the reuse.

Looking at the circuit of Fig.1(a), it is straightforward to conclude that, a fast design strategy, is to define the transistor parameters(V_{ds}, V_{gs}, I_{ds} and L) and then calculate the transistors W and the resistor for a desired transconductance. For the circuit of Fig.1(b), the same operation can be realized, although for this circuit the dimensions of the current source influence in the transconductance, as it can be seen in the Fig.3.

For this strategy to be successful, we need a relationship between the resistor and the desired Gm. This can be made isolating R in equations (4) and (10), resulting in (24) and (25).

If the resistance obtained is negative, it means that the current bias is not high enough for the transconductance required and, in this case, the designer can be warned or opt for an automatic increment of current.

For the active source degeneration topologies, we don't have a simple method, and a few iterations to find an accurate value of Gm are needed. The dependency graph of the MOS degeneration is presented in Fig.5. In the first step, the transistor M_1 is dimensioned with the input parameters (V_{dd}, V_{gs}, L_1 and gm), defined by designer, then CAIRO+ procedure give the transistor width(W_1), the current bias(I_{bias}), the common-source output conductance(Gds) and the parasitic capacitances. After that, the current source can be dimensioned using the current I_{bias} and the its input parameters for this one(V_{bias} and L_2).

For the degeneration pair, we have $V_{ds} = 0$, $I_{ds} = 0$, the same M_1 length (L_1) was used and the width is chosen to conserve the ratio $a = 2.75$ [3].

Once the transistors are sized, the transconductance is calculated and if it is smaller than desired, the gm of the transistor M_1 is increased and the procedure is restarted in order to recalculate all transistors. This operation is repeated until the desired transconductance are found.

IV. Design Examples and Simulation Results

In order to validate the proposed design methodology, spice simulations have been carried out with the circuits given by CAIRO+ for several transconductance values and a constant resistance load for a $130nm$ CMOS technology. The results are shown in table I.

In Fig.6 the transconductance as function at the input differential voltage simulated by spice, is shown. For the third topology, a "hump" can be observed in the middle of the Gm curve. As mentioned in [3], this "hump" is enhanced for higher bias current and can be compensated by adjusting of the parameter "a". Fig.6 also shows the transconductance curve where the parameter "a" is 3.5.

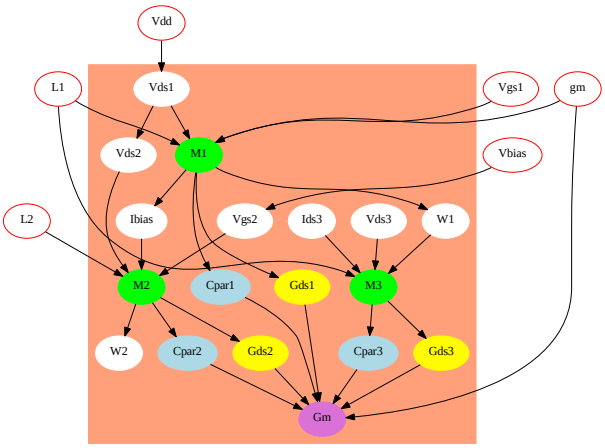

Fig. 5. Dependency graph of the MOS Degeneration

Once the design method is validated, a transconductor of each type was realized with a RLC filter (with center frequency $f_0 = 945Mhz$ and quality factor $Q = 80$) connected at the output. A IP3(Third-order intercept point) simulation is committed in order to compare the performance of the three topologies as shown in Fig.7. In table II the calculated transistors dimensions by CAIRO+ are shown.

TABLE I
SIMULATED TRANSCONDUCTANCE

Gm	Topology		
	1	2	3
1.0e-3 ℧	1.00e-3 ℧	1.00e-3 ℧	9.94e-4 ℧
1.2e-3 ℧	1.22e-3 ℧	1.21e-3 ℧	1.19e-3 ℧
1.5e-3 ℧	1.52e-3 ℧	1.51e-3 ℧	1.56e-3 ℧
2.0e-3 ℧	2.00e-3 ℧	2.00e-3 ℧	2.06e-3 ℧
2.5e-3 ℧	2.51e-3 ℧	2.51e-3 ℧	2.57e-3 ℧
2.7e-3 ℧	2.71e-3 ℧	2.71e-3 ℧	2.79e-3 ℧
3.0e-3 ℧	3.01e-3 ℧	3.01e-3 ℧	3.12e-3 ℧

TABLE II
TRANSISTORS DIMENSIONS CALCULATED BY CAIRO+ FOR A 130 nm TECHNOLOGY ($945Mhz$)

Topology	1	2	3 (a=3.5)
W_1	3.63e-6 m	5.75e-6 m	5.57e-6 m
W_s	267e-6 m	128e-6 m	116e-6 m
W_{deg}	-	-	0.83e-6 m
L_1	1.3e-7 m	1.3e-7 m	1.3e-7 m
L_s	3e-7 m	3e-7 m	3e-7 m
L_{deg}	-	-	1.3e-7 m
V_{ds}	0.6 V	0.7 V	0.7 V
I_{bias}	1.236 mA	1.236 mA	1.236 mA
R_{deg}	283 Ω	1035 Ω	-
G_m	1.08e-3 ℧	1.04e-3 ℧	1.05e-3 ℧

V. CONCLUSION

In this paper we have presented a novel methodology to design linear transconductors in CMOS for three different topologies to be used in a synthesis tool, thereunto a highly accurate small-signal model of theses topologies has been

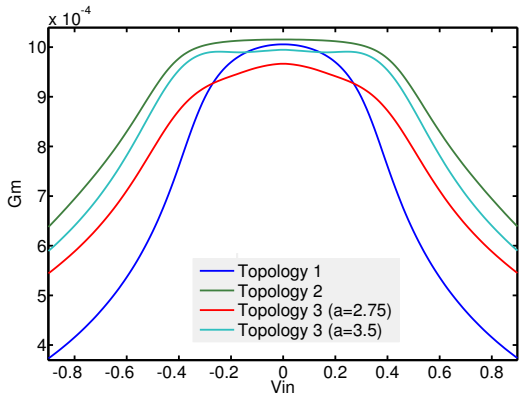

Fig. 6. Small-signal transconductance for different topologies

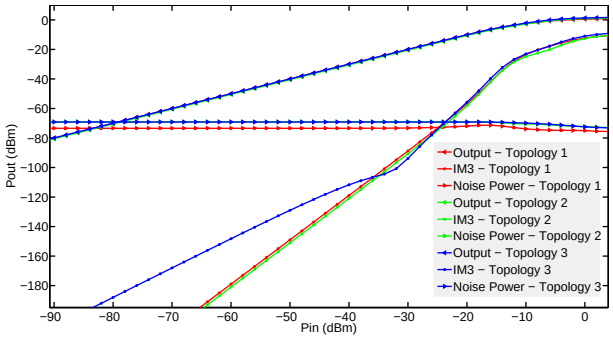

Fig. 7. Output power of fundamental, output noise floor and IM3 versus Input power for the three topologies

studied and analytical expressions for Gm were obtained for each one of them. The simulations results show that the transconductors obtained are very closed to the desired, validating the proposed approach.

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