CCIAC

Conception de Circuits Intégrés Analogique CMOS

Hassan.Aboushady@lip6.fr
http://www-asim.lip6.fr/~hassan

References

• B. Razavi, "Design of Analog CMOS Integrated Circuits", Mc Graw-Hill, 2001.

• K. Martin & D. Johns, "Analog Integrated Circuits Design", John Wiley, 1997.

• W. Sansen & K. Laker, "Design of Analog Integrated Circuits & Systems", Mc Graw-Hill, 1994.

• P. Gray & R. Meyer, "Analysis and Design of Analog Integrated Circuits", third edition, John Wiley 1993.

• G. Temes & R. Gregorian, "Analog MOS Integrated Circuits for Signal Processing", John Wiley, 1986.

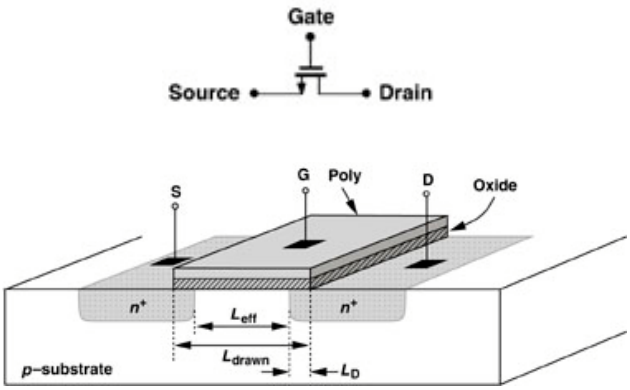
• Jacky Porte,"OCEANE: Outils pour la Conception et l' Enseignement des circuits intégrés ANalogiquEs", *http://www-asim.lip6.fr/recherche/analog/oceane/*

Lecture I
Basic MOS Device Physics

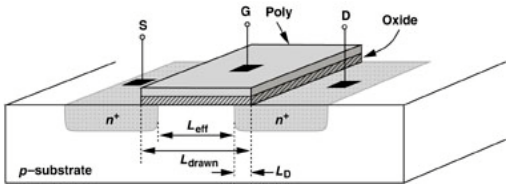
Basic MOS Device Physics

- **The MOSFET structure**
- **MOS I/V Characteristics**
- **Second Order Effects**
- **MOS Device models**

MOS Device Structure



NMOS Structure

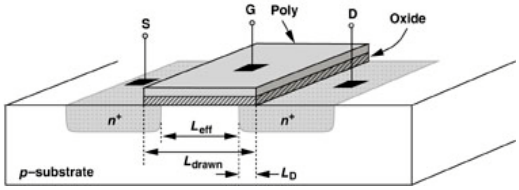


- P-type substrate ("Bulk", "Body")
- D and S heavily doped (n^+) n-regions
- Gate is heavily doped polysilicon (amorphous non-crystal)
- Thin layer of S_iO_2 to insulate Gate from Substrate

Gate Dimensions

- L = Length W = Width
- During fabrication S and D "side diffuse": Actual L is slightly less than the drawn layout L.
  - L_D = Amount of side diffusion
  - L_{Drawn} = Layout intention of L
  - L_{eff} = Effective Length
  - Then: $L_{eff} = L_{Drawn} - 2\,L_D$

Gate Oxide thickness = t_{ox}



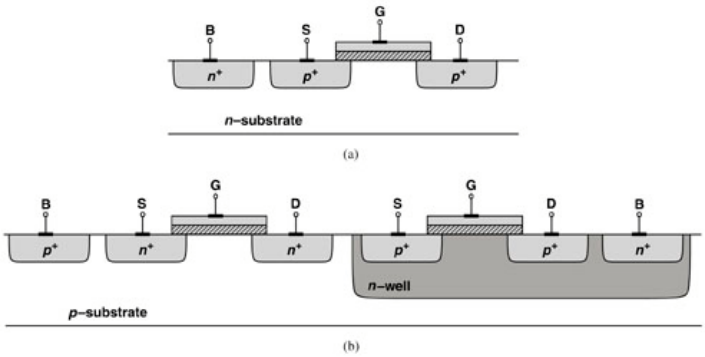
Technology Trends

- The principal thrust in MOS technology is to reduce both L and t_{ox}
- Example:

$$L_{eff} \approx 90\ nm$$

$$t_{ox} \approx 2.5\ nm$$

NMOS and PMOS with Well

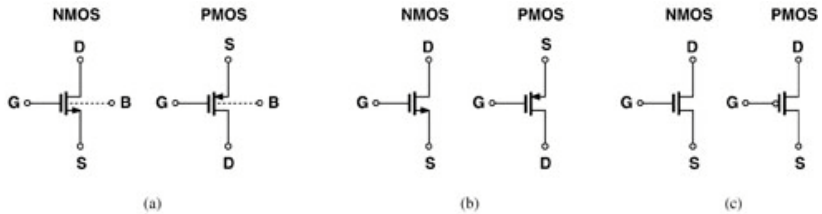


- PMOS fabricated in a "local substrate" called "well"
- All NMOS devices on a chip share the same substrate
- Each PMOS device on a chip has an independent n-well

Carriers & Currents

- Carriers always flow from the Source to Drain
- NMOS: Free electrons move from Source to Drain.
  - ❖ Current direction is from Drain to Source.
- PMOS: Free holes move from Source to Drain.
  - ❖ Current direction is from Source to Drain.

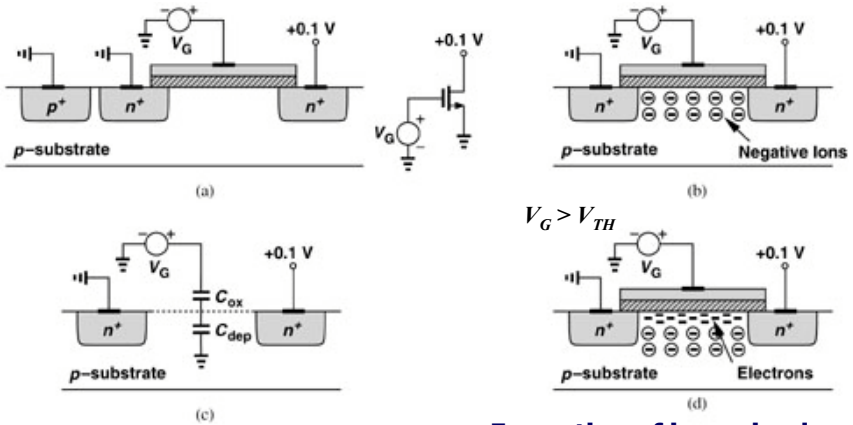
MOS Symbols



- **Symbols (a) are the most general, allowing B to be connected anywhere.**
- **Symbols (b) will be used most frequently: Whenever B of NMOS is tied to GND, or B of PMOS is tied to V_{DD}**
- **Symbols (c) used in digital circuits.**

MOS Channel Formation

Formation of depletion region

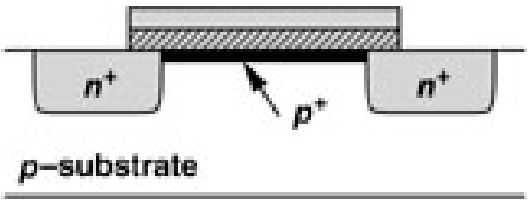


$V_G > V_{TH}$

Formation of inversion layer

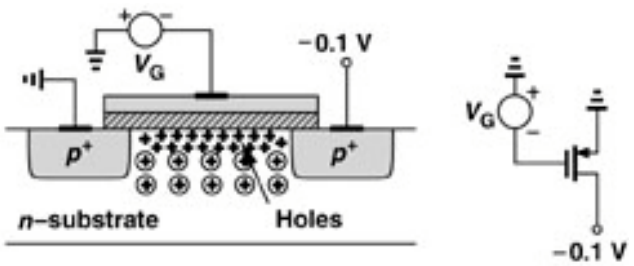
Threshold Voltage V_{TH} Adjustment

- V_{TH} is adjusted by implantation of dopants into the channel area during device fabrication.
- A thin sheet of p+ is created, the gate voltage required to deplete this region increases.



PMOS Channel Formation

- Exactly like NMOS but with all of the polarities reversed.



Basic MOS Device Physics

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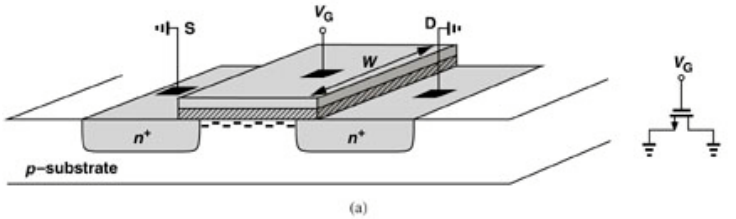
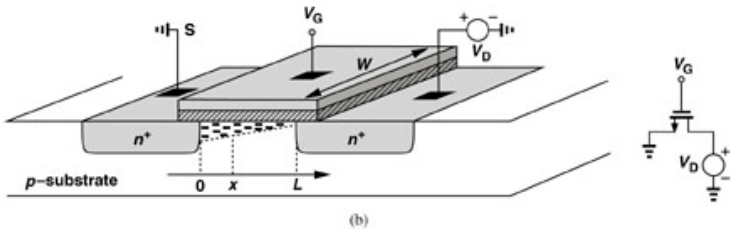
- MOS I/V Characteristics
- Second Order Effects
- MOS Device models

I/V Characteristics

Equal source and drain voltages





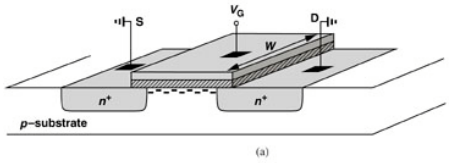
Unequal source and drain voltages

I/V Characteristics

$$I = Q_d \cdot v$$

Uniform channel charge density:

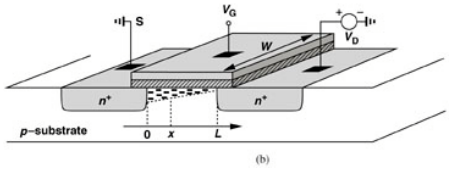
$$Q_d = WC_{ox}(V_{GS} - V_{TH})$$



The local voltage between gate and channel varies:

$$Q_d(x) = WC_{ox}(V_{GS} - V(x) - V_{TH})$$

$$I_D = -WC_{ox}[V_{GS} - V(x) - V_{TH}]\,v$$



Q_d : **charge density (C/m)**

v : **velocity of the charge (m/s)**

WC_{ox} : **total capacitance per unit length**

I/V Characteristics (cont.)

$$I_D = -WC_{ox}[V_{GS} - V(x) - V_{TH}]\,v$$

$$Given\ v = \mu_n E \ and\ E(x) = -\frac{dV(x)}{dx}$$

- μ_n: mobility of electrons
- E: Electric field

$$I_D = WC_{ox}[V_{GS} - V(x) - V_{TH}]\mu_n \frac{dV(x)}{dx}$$

$$\int_{x=0}^{L} I_D\,dx = \int_{V=0}^{V_{DS}} WC_{ox}\mu_n[V_{GS} - V(x) - V_{TH}]\,dV$$

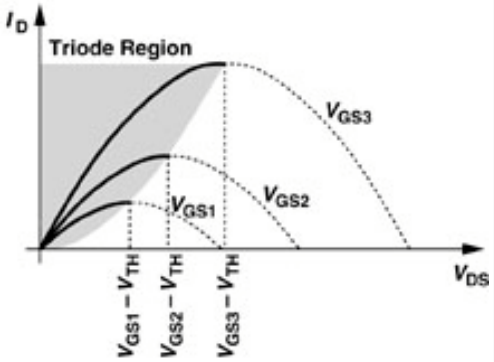
I_D is constant along the channel

$$I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}{V_{DS}}^2\right]$$

I/V Characteristics (cont.)

$$I_D = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]$$

$$I_{D\max} = \frac{\partial I_D}{\partial V_{DS}} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2$$



Triode = Linear = ohmic

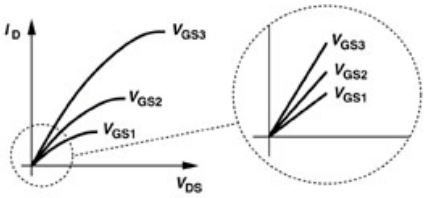
Operation in Triode Region

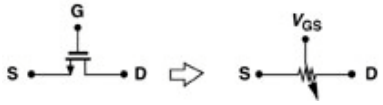
$$I_D = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]$$

$$V_{DS} << 2(V_{GS} - V_{TH})$$

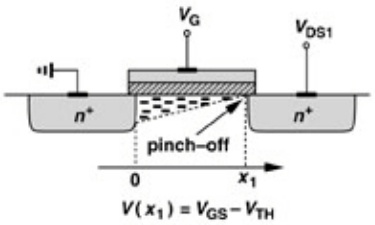
$$I_D \approx \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})V_{DS},$$

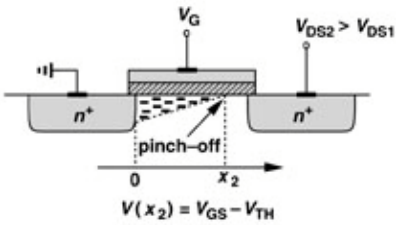
$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$$





Operation in the Saturation Region

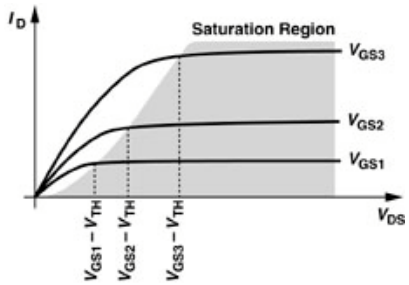




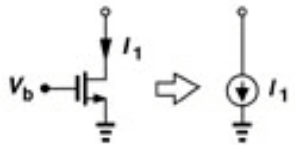
$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

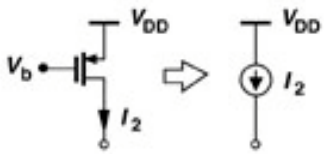
$$V'_{DS} = V_{GS} - V_{TH} \quad (Pinch - off)$$

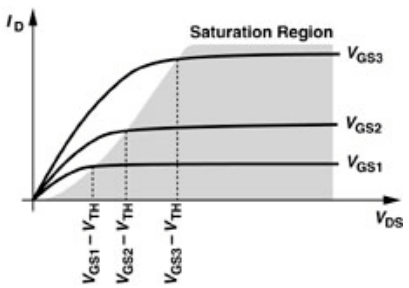
$$\boxed{I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2}$$



Saturated MOS Operating as a Current Source







Transconductance, g_m

MOSFET operating in saturation produces a current in response to its gate-source overdrive voltage.

➡ **The transconductance is a figure of merit that indicates how well a device converts a voltage to current.**

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{VDS\ \text{constant}}$$

W/L Constant | W/L Constant | I_D Constant

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH}) \qquad g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D} \qquad g_m = \frac{2I_D}{V_{GS}-V_{TH}}$$

Basic MOS Device Physics

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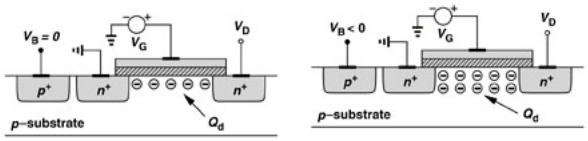
Threshold Voltage and Body Effect



$V_B \downarrow \Rightarrow$ **More holes are attracted to the substrate connection leaving a larger negative charge behind**

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}\right)$$

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_{sub}}}{C_{ox}}$$

$$\Phi_F = \left(kT/q\right)\ln\left(N_{sub}/n_i\right)$$

Threshold Voltage and Body Effect (cont.)

N_{sub}= doping concentrationof the substrate

n_i = intrinsic carrier concentration in silicon

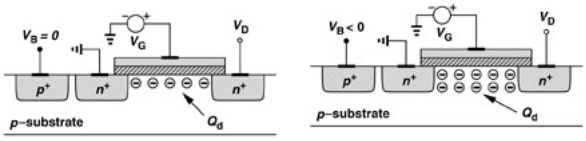
q = electron charge

Φ_F = Fermi-level

C_{ox} = gate oxide capacitance per unit area

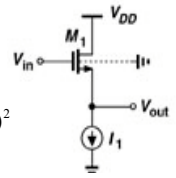
ε_{si} = silicon dielectric constant

Threshold Voltage and Body Effect (cont.)



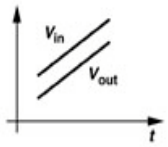
$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}\right)$$

Example:

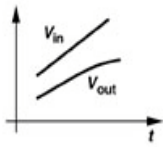


$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{in} - V_{out} - V_{TH})^2$$

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\Phi_F + V_{out}} - \sqrt{2\Phi_F}\right)$$



Without Body Effect



With Body Effect

Bulk Transconductance, g_{mb}

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})\left(-\frac{\partial V_{TH}}{\partial V_{BS}}\right)$$

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{2\Phi_F}\right)$$

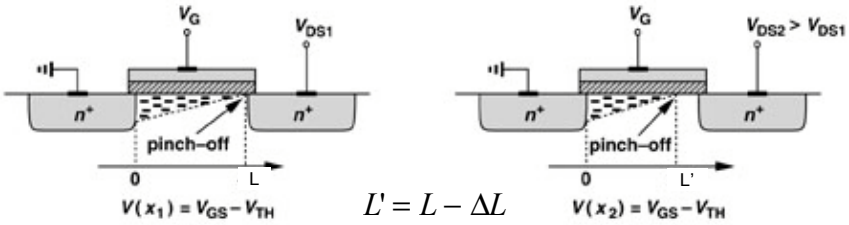
$$-\frac{\partial V_{TH}}{\partial V_{BS}} = \frac{\partial V_{TH}}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}} = \eta$$

$$g_{mb} = g_m \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}}$$

$$= \eta\, g_m$$

$$\frac{\partial V_{TH}}{\partial V_{in}} = \eta\frac{\partial V_{out}}{\partial V_{in}}$$

Channel Length Modulation



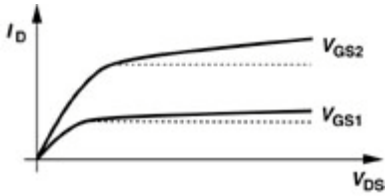
$$L' = L - \Delta L$$

$$\frac{1}{L'} \approx \frac{1}{L}\left(1 + \frac{\Delta L}{L}\right)$$

$$\frac{1}{L'} = \frac{1}{L}(1 + \lambda V_{DS}) \quad where \quad \lambda V_{DS} = \Delta L / L$$

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

Channel Length Modulation (cont.)



$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

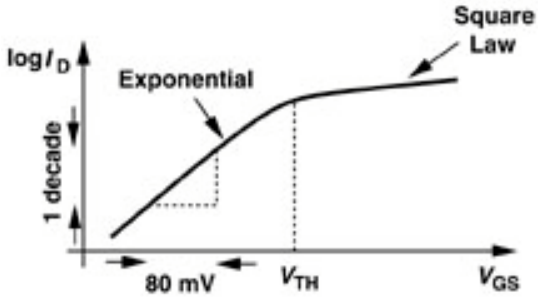
$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})(1 + \lambda V_{DS})$$

$$g_m = \sqrt{\frac{2\mu_n C_{ox} W/L\, I_D}{(1 + \lambda V_{DS})}} \qquad g_m = \frac{2I_D}{V_{GS} - V_{TH}}, \quad (unchanged)$$

Subthreshold Conduction

$$I_D = I_0 \exp\left(\frac{V_{GS}}{\zeta kT/q}\right)$$

Weak Inversion



Significant current leakage for low V_{TH} !

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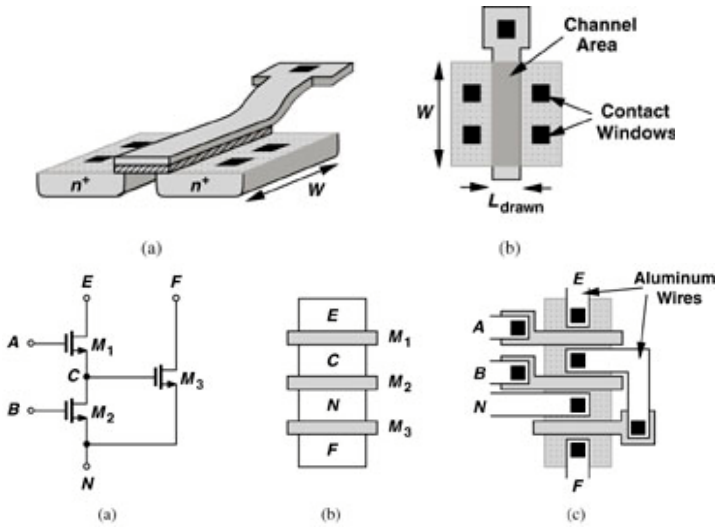
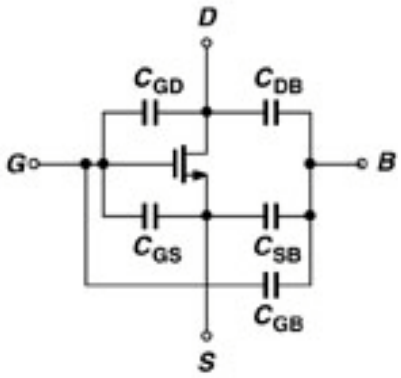
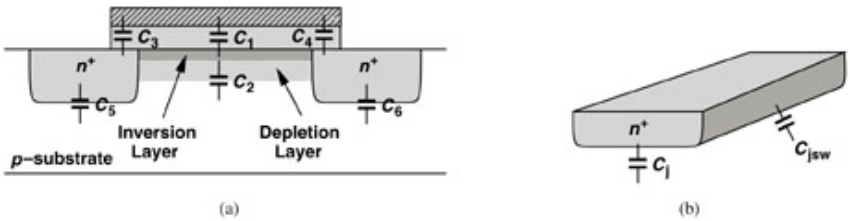
MOS Layout



Device Capacitances



Device Capacitances



C_1 : Oxide capacitance between gate & channel

C_2 : Depletion capacitance between channel & substrate

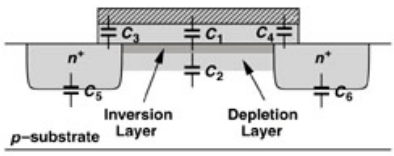
C_3 , C_4 : Overlap of the gate poly with source and drain areas

C_5, C_6 : Junction capacitance between source/drain areas and substrate

Gate-Source and Gate-Drain Capacitance

Device OFF

$$\Rightarrow C_{GD} = C_{GS} = C_{ov}W$$

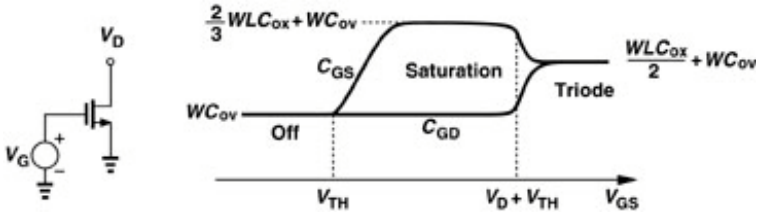


linear region $V_S \approx V_D$

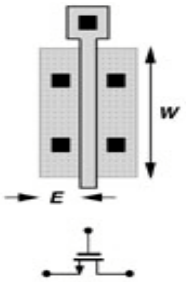
$$\Rightarrow C_{GD} = C_{GS} = \frac{WLC_{ox}}{2} + C_{ov}W$$

saturation region

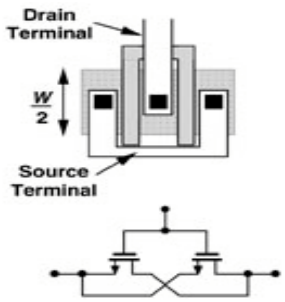
$$\Rightarrow C_{GD} = C_{ov}W \quad \text{and} \quad C_{GS} = \frac{2}{3}WLC_{ox} + C_{ov}W$$



Layout for Low Capacitance



(a)



(b)

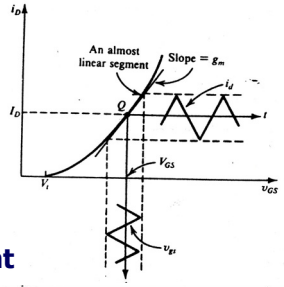
$$C_{DB} = C_{SB} = W\,E\,C_j + 2(W+E)C_{jsw}$$

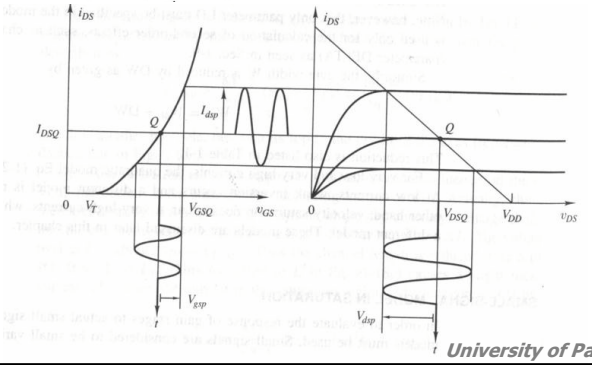
$$C_{DB} = \frac{W}{2}E\,C_j + 2\left(\frac{W}{2}+E\right)C_{jsw}$$

$$C_{SB} = 2\,C_{DB}$$

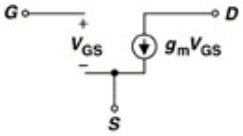
MOS Small Signal Model

Definition:
A linear approximation of the large signal model around the operating point

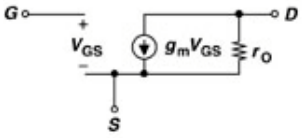




MOS Small Signal Model



Basic MOS small signal model



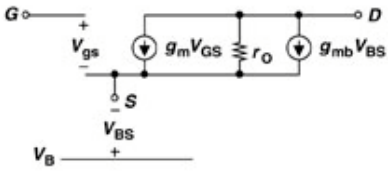
Channel length modulation represented by r_o

$$r_o = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\partial I_D / \partial V_{DS}}$$

$$\boxed{r_o = \frac{1}{\frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2 \lambda} \approx \frac{1}{\lambda I_D}}$$

MOS Small Signal Model

Body effect represented by a dependent current source

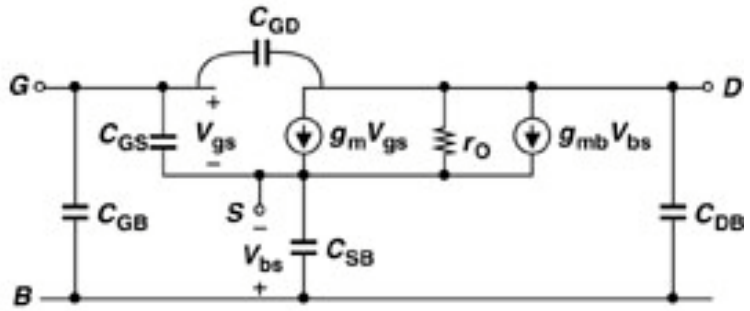


$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})\left(\frac{-\partial V_{TH}}{\partial V_{BS}}\right)$$

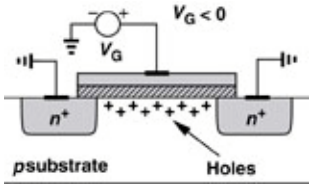
$$\frac{\partial V_{TH}}{\partial V_{BS}} = \frac{-\partial V_{TH}}{\partial V_{SB}} = -\frac{\gamma}{2}(2\Phi_F + V_{SB})^{-1/2}$$

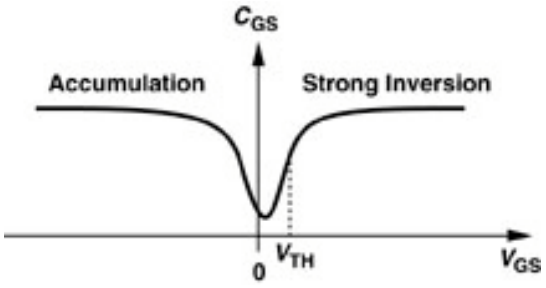
$$\boxed{g_{mb} = g_m \frac{\gamma}{2\sqrt{2\Phi_F + V_{SB}}} = \eta g_m}$$

MOS Small Signal Model with Capacitance



MOS Capacitors are nonlinear





SPICE: "Simulation Program with Integrated Circuit Emphasis"

Level 1 SPICE Models for NMOS and PMOS Devices.

NMOS Model			
LEVEL = 1	VTO = 0.7	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08e−6	UO = 350	LAMBDA = 0.1
TOX = 9e−9	PB = 0.9	CJ = 0.56e−3	CJSW = 0.35e−11
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e−9	JS = 1.0e−8
PMOS Model			
LEVEL = 1	VTO = −0.8	GAMMA = 0.4	PHI = 0.8
NSUB = 5e+14	LD = 0.09e−6	UO = 100	LAMBDA = 0.2
TOX = 9e−9	PB = 0.9	CJ = 0.94e−3	CJSW = 0.32e−11
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e−9	JS = 0.5e−8

VTO: threshold voltage with zero V_{SB} (unit: V)
GAMMA: body effect coefficient (unit: $V^{1/2}$)
PHI: $2\Phi_F$ (unit: V)
TOX: gate oxide thickness (unit: m)
NSUB: substrate doping (unit: cm^{-3})
LD: source/drain side diffusion (unit: m)
UO: channel mobility (unit: $cm^2/V/s$)
LAMBDA: channel-length modulation coefficient (unit: V^{-1})
CJ: source/drain bottom-plate junction capacitance per unit area (unit: F/m^2)
CJSW: source/drain sidewall junction capacitance per unit length (unit: F/m)
PB: source/drain junction built-in potential (unit: V)
MJ: exponent in CJ equation (unitless)
MJSW: exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit: F/m)
CGSO: gate-source overlap capacitance per unit width (unit: F/m)
JS: source/drain leakage current per unit area (unit: A/m^2)