CMOS Process Technology

- *General Layout Considerations*
- *Wafer Processing*
- *Photolithography*
- *Oxidation*
- *Ion Implantation*
- *Deposition and Etching*
- *Device Fabrication.*

Hassan Aboushady
University of Paris VI

References

- **B. Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill, 2001.**

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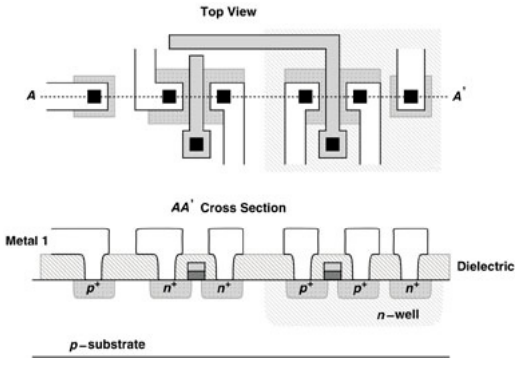
Hassan Aboushady
University of Paris VI

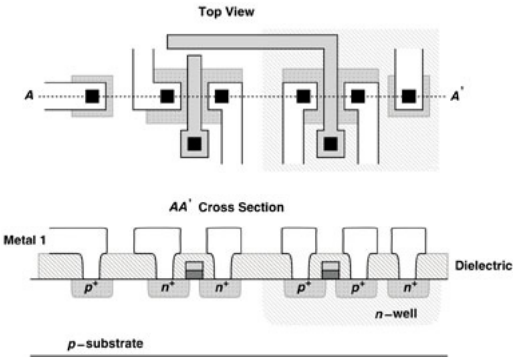
General Considerations



- How are various regions defined so accurately ?
- How are nwells and Source/Drain regions built ?
- How are the gate oxide and polysilicon aligned with Source/Drain regions ?
- How are the contact window created?
- How are the metal interconnect layers deposited?

Modern CMOS technologies involve more than 200 processing steps !

General Considerations



(1) Wafer processing to produce the proper type of substrate.

(2) Photolithography to precisely define each region.

(3) Oxidation, deposition and ion implantation to add materials to the wafer.

(4) Etching to remove materials from the wafer.

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Hassan Aboushady
University of Paris VI

Wafer Processing

- **The starting wafer in a CMOS technology must be created with a very high quality.**
- **The wafer must be grown as a single crystal silicon body having a very small number of "defects", dislocations or impurities.**
- **The wafer must contain the proper type and level of doping so as to achieve the required resistivity.**
- **In most CMOS technologies, the wafer has a resistivity of 0.05 to 0.1 Ω.cm and a thickness of 500 to 1000 μm, which reduces to a few hundred microns after all of the processing steps.**

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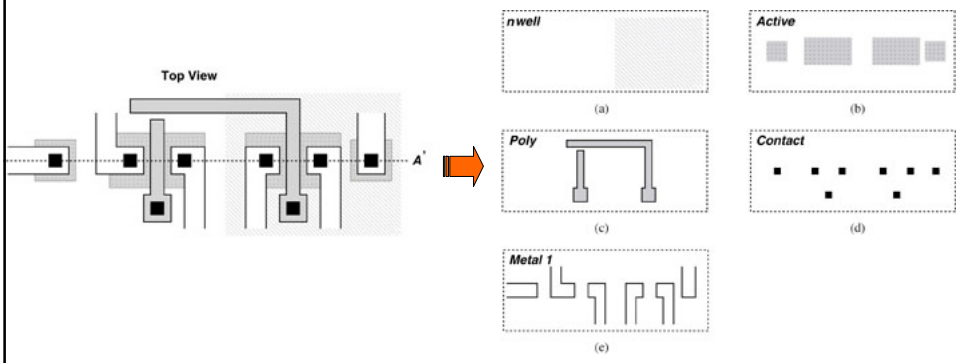
Photolithography

The first step in transferring circuit layout information to Wafer.

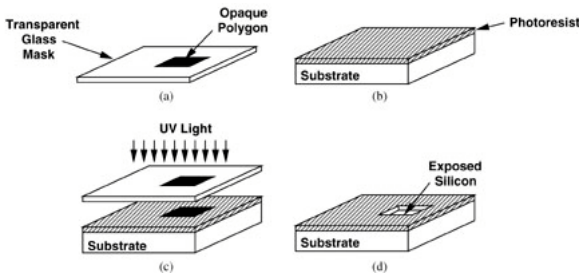


Photolithography example: the n-well pattern

(a) The pattern is written to a transparent glass mask by a precisely controlled electron beam.

(b) The wafer is covered by a thin layer of photoresist, a material whose etching properties change upon light exposure.

Lithography Sequence



(c) The mask is placed on top of the wafer and the pattern is projected onto the wafer by UV light.

(d) The wafer is placed in an etchant that dissolves the "soft" photoresist area.

Photolithography Cost

2 types of photoresists:

- **positive: hardens in areas NOT exposed to light.**
- **negative: hardens in area exposed to light.**

Cost of fabrication α number of masks in a process

Lithography is a slow and expensive task.
Each mask costs several thousand $

- **Historically CMOS, low cost process: only 7 masks.**

- **New CMOS process: 25 masks, but still low cost because both number of transistors per unit area and the size of the wafer has significantly increased.**

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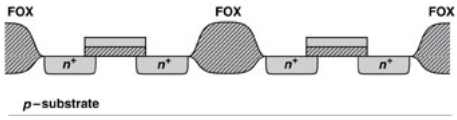
University of Paris VI

Oxidation



Purpose:
(1) A thin layer of SiO_2 for Gate-oxide layers: tox = few nanometers.

(2) A thick layer SiO_2 ,called "Field Oxide" (FOX), in areas between devices. Provides foundation for interconnect lines.

Fabrication:
Silicon Dioxide is grown by placing the exposed silicon in an oxidizing atmosphere such as oxygen at a temperature around 1000°C.

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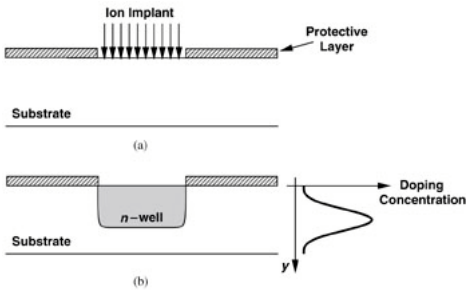
University of Paris VI

Ion Implantation

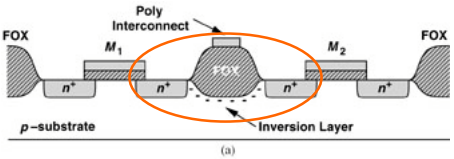


Doping atoms are accelerated as a high energy focused beam, hitting the surface of the wafer and penetrating the exposed areas.

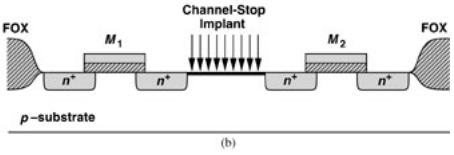
- **Doping level: is determined by the intensity and duration of the implantation.**
- **Depth of doped region: is set by the energy of the beam.**

"Channel Stop" Regions

MOS transistor with thick gate oxide :
leakage path between M1 & M2.



Channel Stop implant before FOX is grown to to raise V_{TH} to a very large value.

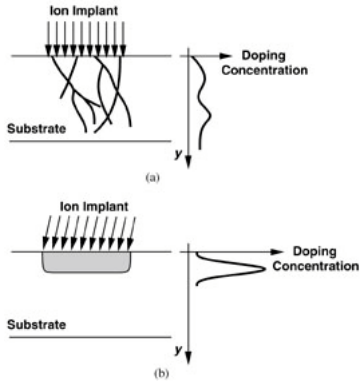


Annealing: ion implantation damages the silicon lattice extensively. The wafer is heated to 1000°C for 15~30 mn to allow the lattice bonds to form again.
(This operation results in side-diffusion of Source/Drain regions, creating overlap with the gate area.)

Channeling

If beam implant is aligned with crystal axis, the ions penetrate the wafer to a great depth.

➡ The implant is tilted by 7-9°.



Impacts matching of transistors
➡ necessitating precautions in the layout

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Hassan Aboushady
University of Paris VI

CMOS Process Technology

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Hassan Aboushady
University of Paris VI

Basic Transistor Fabrication

(a) A thin layer of SiO_2 is grown as a protective coating.

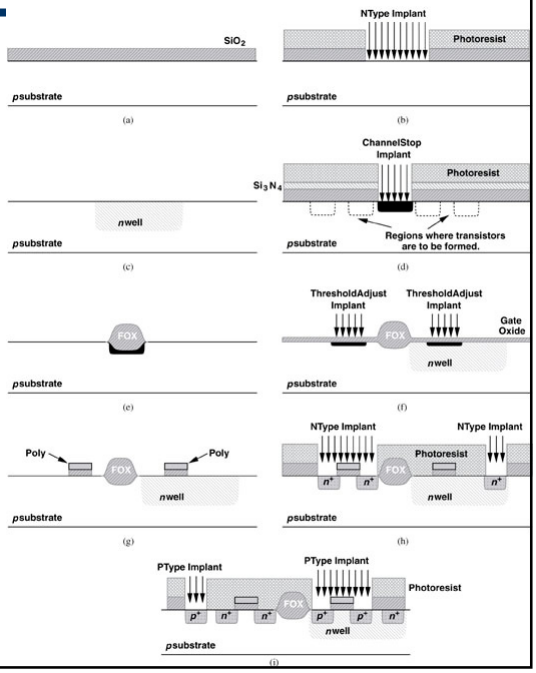
(b) Lithography sequence.
(c) clean up.

(d) Channel-Stop implant and FOX grown.
(e) clean up

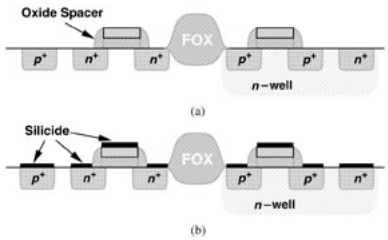
(f) Growth of gate-oxide and V_{TH} adjustment.

(g) polysilicon layer is deposited.

(h) N+ implant.
(i) P+ implant.



"Silicidation"



Sheet resistance of doped polysilicon and Source/Draon regions is typically several tens of ohms per square.

Silicidation: covering polysilicon and active areas with highly conductive material (titanium silicide).

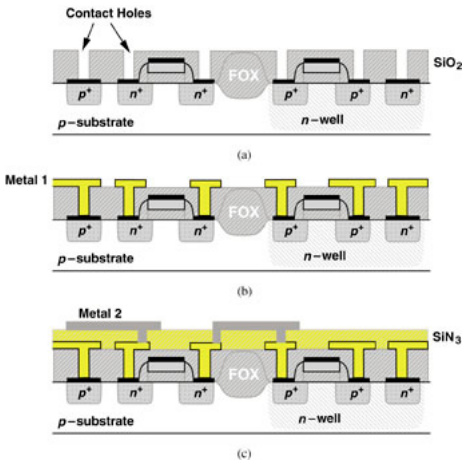
Oxide Spacer: to avoid the silicide layer on the gate to be shorted to that on the Drain/Source.

Contact and Metal Fabrication

(a) - Cover the wafer with a thick layer of oxide.
- Lithography sequence using the contact mask.
- Contact holes are created by plasma etching.

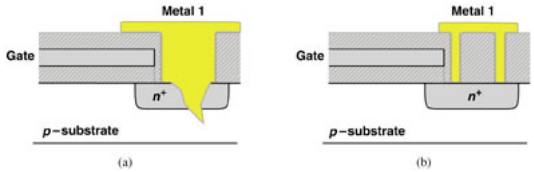
(b) - Metal 1 is deposited over the entire wafer.
- Lithography sequence using the Metal 1 mask.
- Etching

(c) Same as (b) with metal 2.



Each metal layer requires 2 masks: - 1 mask for the contacts
- 1 mask for the metal

"Spiking"



(a) Spiking due to large contact areas.

(b) Use of small contacts to avoid spiking.

Layout and Mismatch

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- Analog Layout Techniques
- Substrate Coupling

Hassan Aboushady
University of Paris VI

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Recent CMOS processes

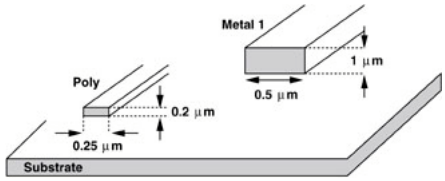
Device Scaling has increased speed of transistors.

- **Unwanted interaction between different sections of integrated circuits.**
- **Non-idealities in layout and packaging limit both the speed and precision of such systems.**

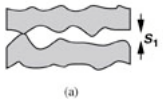
Design Rules: Minimum Width, Spacing

Minimum Width
imposed by lithography & processing capabilities

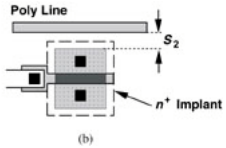
Minimum Width α Layer Thickness



Minimum Spacing
if too close ⇨ they may be shorted

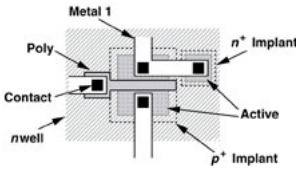


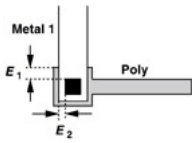
Minimum Spacing
between active and poly



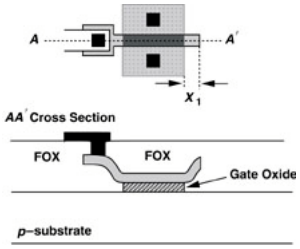
Design Rules: Minimum Enclosure, Extension

Minimum Enclosure
- **nwell and p+ implant must surround the PMOS transistor with sufficient margin.**
- **To ensure that the contact remains inside the poly and metal 1 squares, both geometries must enclose the contact with enough margin.**



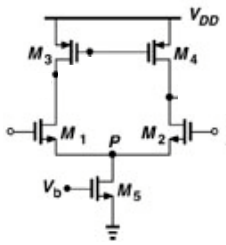


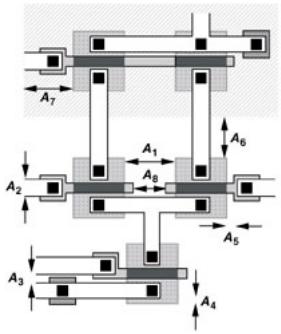
Minimum Extension
- **Some geometries must extend beyond the edge of others by a minimum value.**



FOX : A Thick layer of SiO_2

Ex: Differential Pair with PMOS current-source load



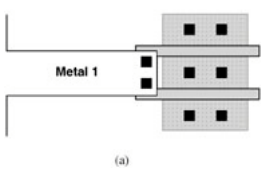


A_1: Active–Active Spacing
A_2: Metal Width
A_3: Metal–Metal Spacing
A_4: Enclosure of Contact by Active
A_5: Poly–Active Spacing
A_6: Active–Well Spacing
A_7: Enclosure of Active by Well
A_8: Poly–Poly Spacing

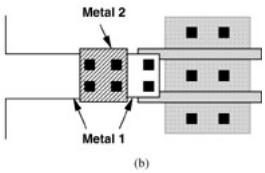
Antenna Effect

During etching, metal area acts as an "antenna" collecting ions, and rising in potential.

⇨ Possible increase of MOS gate voltage to the point that gate-oxide breaks down during fabrication.



Layout susceptible to antenna effect



Discontinuity in metal 1 layer to avoid antenna effect.

Layout and Mismatch

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- *Substrate Coupling*

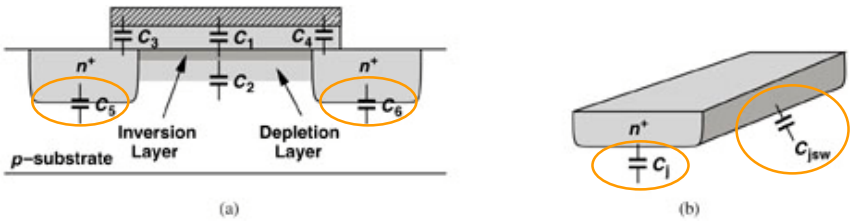
Hassan Aboushady
University of Paris VI

Analog Layout Techniques

- CMOS processes aim to maximize the yield of digital ICs.

- Analog systems demand many more layout precautions so as to minimize effects such as:
  - Crosstalk
  - Mismatch
  - Noise
  - ...

MOS Transistor Parasitic Capacitances



C_1 : Oxide capacitance between gate & channel

C_2 : Depletion capacitance between channel & substrate

C_3 , C_4 : Overlap of the gate poly with source and drain areas

C_5, C_6 : Junction capacitance between source/drain areas and substrate

Folding Reduces S/D Junction Area and Gate Resistance

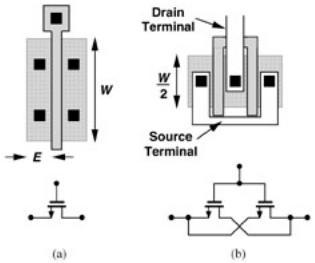
Source/Drain Junction Capacitances:

- **1 finger :**

$$C_{DB} = C_{SB} = W\,E\,C_j + 2(W+E)C_{jsw}$$

- **2 fingers :**

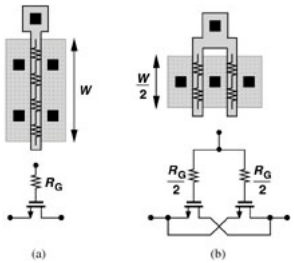
$$C_{DB} = \frac{W}{2}E\,C_j + 2\left(\frac{W}{2}+E\right)C_{jsw}$$
$$C_{SB} = 2\,C_{DB}$$



Gate Resistance:

- **1 finger :** $R = R_G$

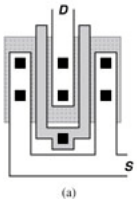
- **2 fingers :** $R = \frac{R_G}{4}$



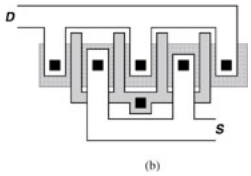
Multi-Finger Transistors

S/D perimeter capacitance for an odd number of fingers N:

$$C_P = \frac{N+1}{2}\left(2E + \frac{2W}{N}\right)C_{jsw}$$
$$= \left[(N+1)E + \frac{N+1}{N}W\right]C_{jsw}$$



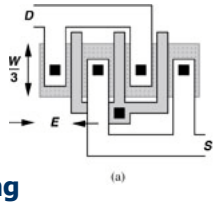
2 fingers



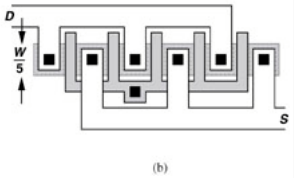
4 fingers

To minimize S/D perimeter capacitance contribution:

$$N\,E << W$$



3 fingers



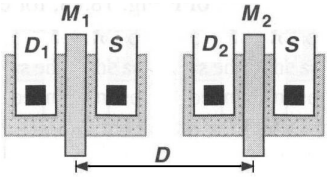
5 fingers

May conflict with minimizing gate resistance.

Transistors Matching

- **Pelgrom: « for each parameter P in any two separate transistors, there exists a fixed part and a randomly varying part which can be represented by a random variable ΔP such that**

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D^2$$



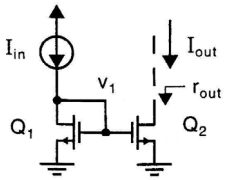
where A_P and S_P are process dependent constants,
W and L are transistor dimensions, and
D is the separation between the two transistors »

➡ **For matched transistors, we must use large devices placed close to each other.**

M. Pelgrom *et. al.* , «Matching Properties of MOS transistors », IEEE JSSC, Vol. 24, No. 5, October 1989

Current Mirrors

- Transistor Q_1 is a diode-connected transistor.



$$\frac{I_{out}}{I_{in}} = \frac{\mu_{n2} C_{ox2} \frac{W_2}{L_2} (V_{GS2} - V_{TH2})^2 (1 + \lambda V_{DS2})}{\mu_{n1} C_{ox1} \frac{W_1}{L_1} (V_{GS1} - V_{TH1})^2 (1 + \lambda V_{DS1})}$$

- For two perfectly matched transistors: $\frac{I_{out}}{I_{in}} = \frac{W_2/L_2}{W_1/L_1}$
- Due to random process variations of
  - V_{TH} as a result of differences of oxide thickness, doping, ...
  - β as a result of differences in W, L, oxide thickness and mobility

  on the same chip: $\Delta I = \frac{\partial I}{\partial \beta} \Delta\beta + \frac{\partial I}{\partial V_{TH}} \Delta V_{TH}$

Current Mirrors

- ➡ $\frac{\Delta I}{I} = \frac{\Delta\beta}{\beta} - \frac{g_m}{I} \Delta V_{TH}$
- This variations (ΔV_{th} and $\Delta\beta$) are modeled as random variables
  - $\sigma_{th} = \sigma(\Delta V_{th}) \approx 10 - 25$ mV
  - $\sigma_{\beta} = \sigma(\Delta\beta/\beta) \approx 0.1 - 10$ %
- Assuming that they are statistically independent (uncorrelated) !!

$$\sigma\left(\frac{\Delta I}{I}\right) = \sqrt{\sigma_\beta^{\,2} + \left(\frac{2}{(V_{GS} - V_{TH})} \sigma_{th}\right)^2}$$

- This error can be made small by
  - ➡ biasing the transistors deeply in strong inversion, (high $V_{GS} - V_{th}$).
  - ➡ using closely placed transistors in the layout to reduce random variations.

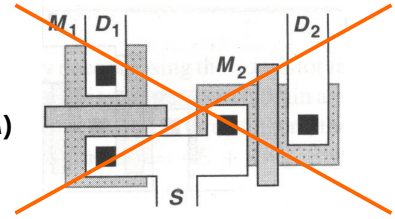
Transistor Mismatch: Orientation

Ex: differential pair **which layout ?**

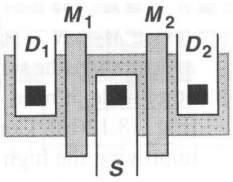
Different Orientations !

ω

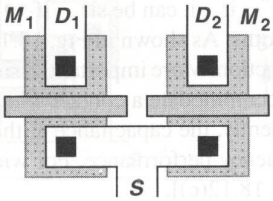
(A)



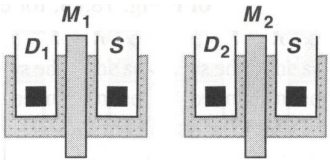
(B)



(C)

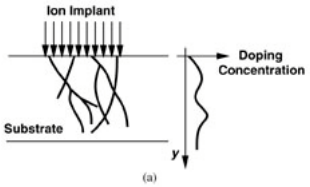


(D)

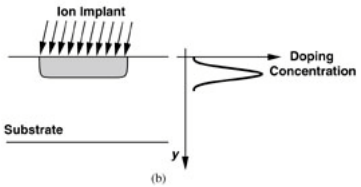


Mismatch Effects: Shadowing

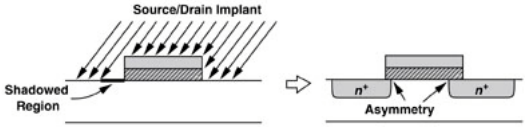
- **During source/drain implantation, if the implant beam is aligned with the crystal axis, the ions penetrate the wafer to a great depth.**



- **Wafer implant is tilted by about 7° to avoid channeling.**

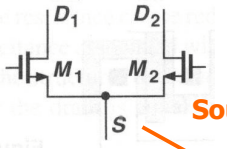


- **Asymmetry between the source and drain diffusion after annealing.**

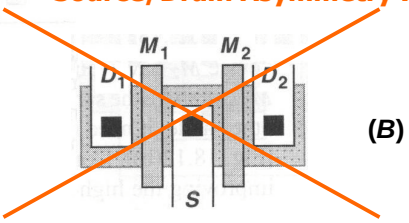


Transistor Mismatch: Shadowing

Ex: differential pair **which layout ?**

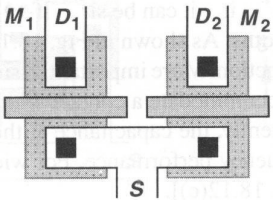


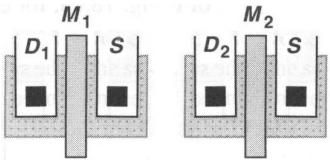
Source/Drain Asymmetry !



(B)

(C)



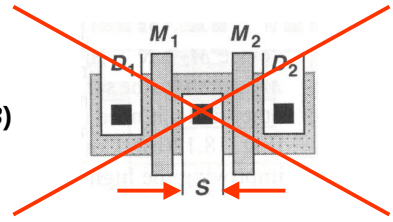


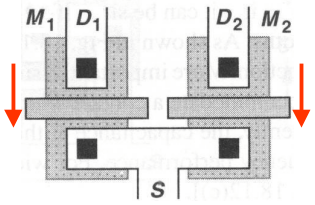
(D)

Transistor Mismatch: Current Orientation

- Due to silicon crystal anisotropy, the current is not exactly the same in all directions.
- Dummy transistors are inserted to control current orientation while minimizing layout area.

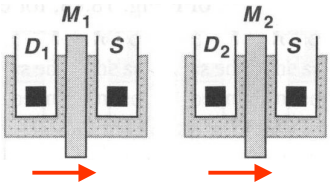
(B)

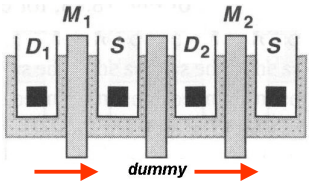




(C)

(D)





(E)

Transistor Mismatch: Boundary Effect

- During polysilicon etching, it continues to cut under the photoresist (undercut).
- It depends on the boundary, such that the undercut is deeper for free space around the gate, affecting gate length.
- Dummy transistors are inserted at the boundary.

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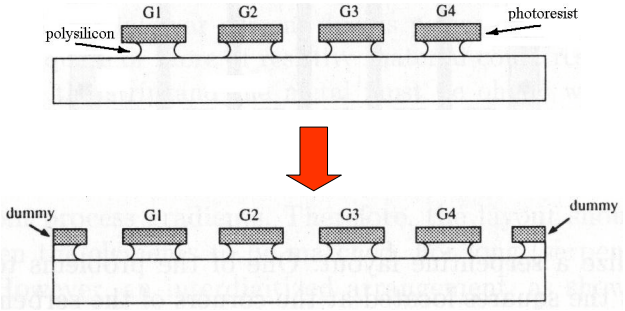
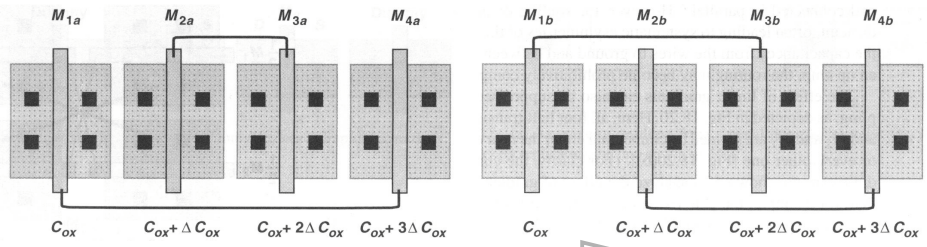


Transistor Mismatch: Gradient Effect

Interdigitization



(A) **Oxide Gradient** **(B)**

- Solution (A): $I_{D1a} + I_{D4a} = \frac{1}{2}\mu_n(C_{ox} + C_{ox} + 3\Delta C_{ox})\frac{W}{L}V_{GST}^2$

  $I_{D2a} + I_{D3a} = \frac{1}{2}\mu_n(C_{ox} + \Delta C_{ox} + C_{ox} + 2\Delta C_{ox})\frac{W}{L}V_{GST}^2$

- Solution (B): $I_{D1b} + I_{D3b} = \frac{1}{2}\mu_n(C_{ox} + C_{ox} + 2\Delta C_{ox})\frac{W}{L}V_{GST}^2$

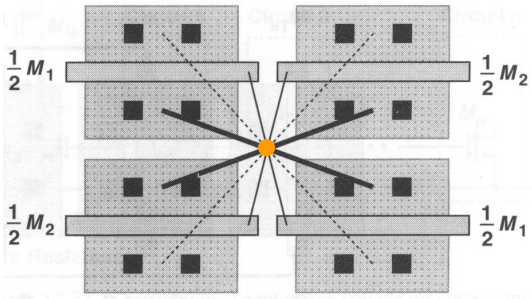
  $I_{D2b} + I_{D4b} = \frac{1}{2}\mu_n(C_{ox} + \Delta C_{ox} + C_{ox} + 3\Delta C_{ox})\frac{W}{L}V_{GST}^2$

Better Matching

Transistor Mismatch: Gradient Effect

Common Centroid

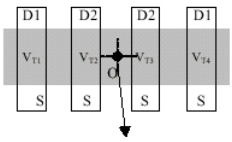
- the effect of 1st order gradients along both axes is cancelled.
- Complex routing leading to asymmetries and parasitic capacitances



Matching Techniques: Comparison

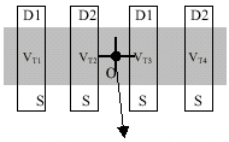
Interdigitized

Type I



Reference coordinate origin

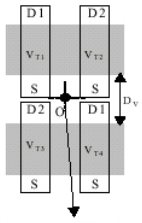
Type II



Reference coordinate origin

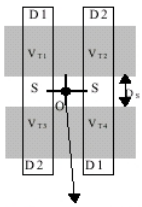
Common Centroid

Type I

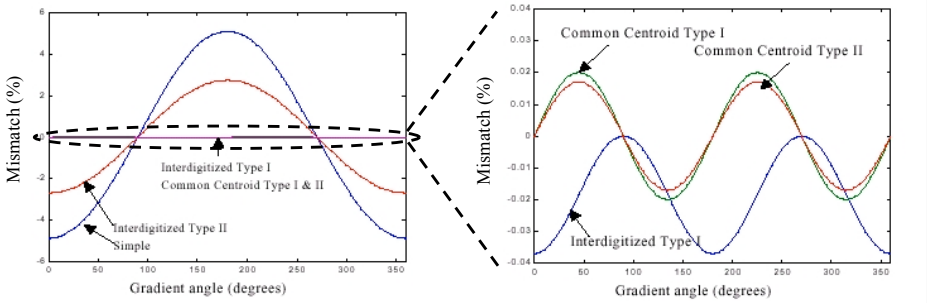


Reference coordinate origin

Type II



Reference coordinate origin



M.- F. Lan *et. al.* , « Current Mirror Layout Strategies for Enhancing Matching Performance », Kluwer AICSP, July 2001.

Interconnects

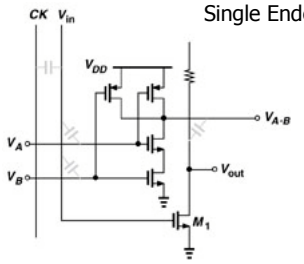
Cross-talk

- **Each coupling capacitance may considerably corrupt Vin or Vout.**

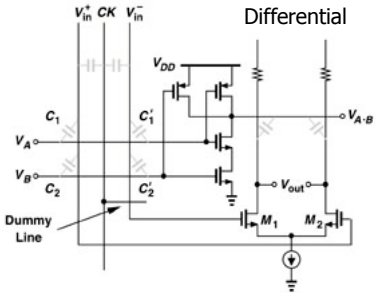
To reduce Cross-talk effect

- **Use differential signals.**
- **Shield sensitive signals.**

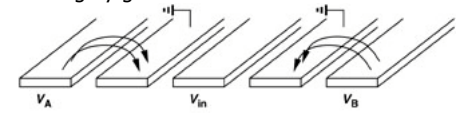
Single Ended



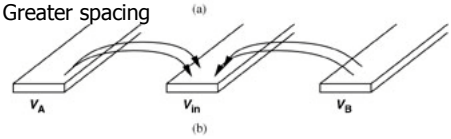
Differential



Shielding by ground lines



Greater spacing



Layout and Mismatch

- ***General Layout Considerations***
- ***Analog Layout Techniques***
- ***Substrate Coupling***

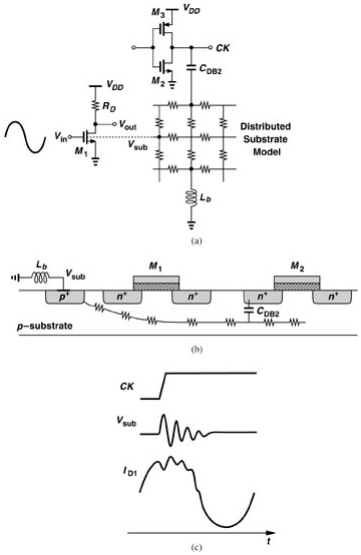
Hassan Aboushady
University of Paris VI

Substrate Coupling

The problem

- **Low resistivity of the substrate creates unwanted paths between various devices in the circuit**

➡ **Corruption of sensitive signals.**



Guard rings

- **Isolates the sensitive circuit from the substrate noise produced by other sections.**