# A 3mW, 250 MSamples/sec, 4-bit Current-Mode FLASH Analog-to-Digital Converter.

J. Bonan, H. Aboushady and M.M. Louërat
*University of Paris VI, LIP6-ASIM Laboratory,*
*4, Place Jussieu, 75252 Paris Cedex 05, France.*
Hassan.Aboushady@lip6.fr

## Abstract

*In this paper, we present a 4-bit FLASH A/D converter. The converter is based on a current mode comparator. In order to increase its sensitivity, the latch following the comparator is in an unstable state during the evaluation phase. The circuit is designed in a 0.18 μm CMOS process, with a supply voltage of 1.8V. Simulation results show that, with a power consumption of 3mW, the sampling frequency reaches 500 MHz.*

## 1. Introduction

Current comparators have been widely used in RAM memories [1][2][3]. Recently, current-mode comparators have been used to implement analog to digital converters [4] [5]. In this paper, we propose an architecture for FLASH A/D converters based on a current-mode comparator.

A general architecture of the proposed current-mode FLASH A/D converter is presented in section 2. In section 3, we describe the operation of the current mode comparator and the transistor sizing optimization for minimum response time. In section 4, we show how the SR latch circuit is used to amplify the comparator output before latching the comparison result. Simulation results are given in section 5 and the conclusion in section 6.

## 2. Current-Mode FLASH Architecture

Figure 1 shows the general architecture of an $N$-bit current-mode FLASH A/D converter. It is composed of $2^N - 1$ current-mode comparators. The $2^N - 2$ reference currents of the converter are realized using NMOS current mirrors for negative reference currents and PMOS current mirrors for positive reference currents. The different values of the reference currents are obtained by varying the $W_p/W_n$ ratios of the current mirrors. Note that the reference current for the level $2^{N-1}$ is nul.

The input signal is copied and distributed to all the comparators using identical current mirrors. Care must be taken in the design of these current mirrors. In fact, harmonic distortion resulting from the non-linearity of these current mirrors has to be below the quantization noise level of the FLASH A/D converter.
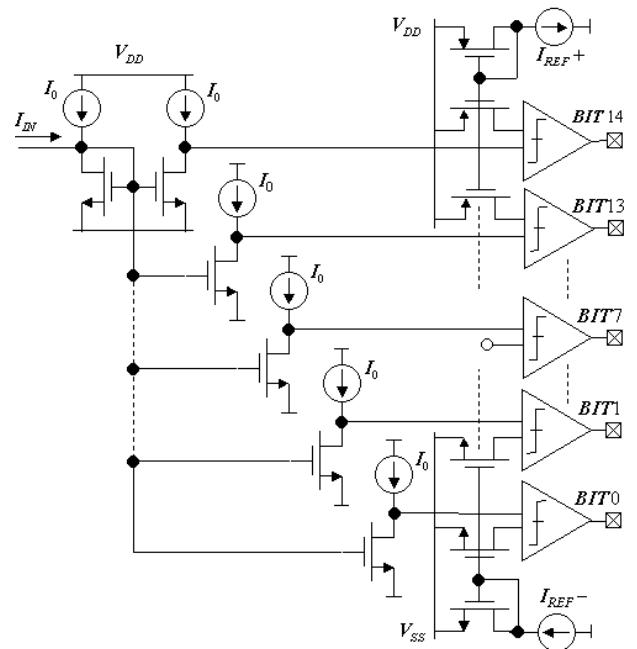


Figure 1. Current-Mode FLASH A/D Architecture.

## 3. The Current-Mode Comparator

### 3.1. Basic Operation

Figure 2 shows the current-mode comparator circuit. This circuit is similar to the comparator presented in [2]. It is constituted of 2 current mirrors and a CMOS latch. The input currents to be compared, $I_{in+}$ and $I_{in-}$, are delivered to the CMOS latch through the cascode current mirrors (M5,M55,M55c) and (M6,M66,M66c). The current sources of this circuit are realized using the transistors (M55p,M55cp) and (M66p,M66cp). These transistors are biased in the saturation region in order to deliver a biasing current $I_0$. The transistors (M55,M55c) and (M66,M66c) are biased in such a way to remain in the saturation region even for a large modulation index [6]. The modulation index $m$ is defined as the ratio of the input current $I_{in}$ over the biasing current $I_0$:
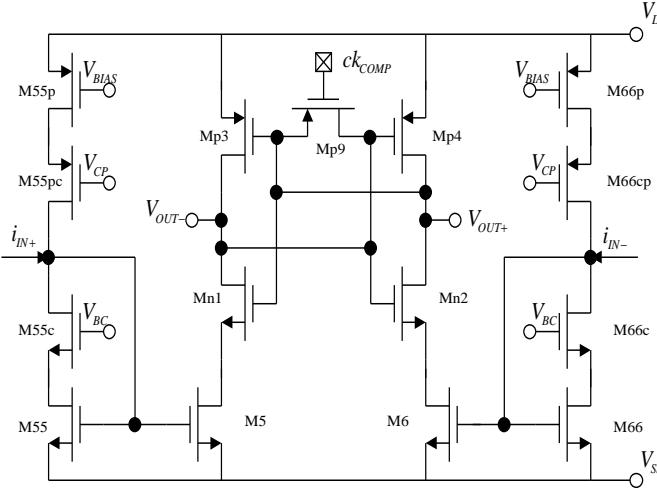
$$m = I_{in}/I_0 \tag{1}$$

Figure 2. The current-mode comparator.



Figure 3. The Gain Bandwith product (GBW) of the CMOS latch (Mn1,Mn2,Mp3,Mp4) in function of the ratio $W_p/W_n$ ($L_n = L_p = L_{min} = 0.18\mu m$). Transistors M5 and M6 are biased for $I_0 = 20\mu A$.

The CMOS latch, shown in Fig.2, is constituted of 2 cross-coupled CMOS inverters (Mn1,Mp3) and (Mn2,Mp4). This latch creates a positive feedback that amplifies the difference between the input currents injected by the transistors (M5,M6). This amplification process occurs in 2 phases: a RESET phase and an EVALUATION phase. During the RESET phase, the clock signal $CK_{COMP}$ is low and the transistor (Mp9) equalizes the currents in the output branches and stabilizes the output at the metastable voltage, $V_m$, which occurs when $V_{out+} = V_{out-}$. The CMOS latch is then in a metastable state. During the evaluation phase, the clock signal $CK_{COMP}$ is high and the difference between the currents flowing in M5 and M6 is amplified by the positive feedback of the CMOS latch. The nodes $V_{out+}$ and $V_{out-}$ are the output voltages of the CMOS latch resulting from the amplification of the difference between in the input currents.

### 3.2. Comparator Optimization

The response time of the comparator determines the maximum sampling frequency of the A/D converter. Optimizing the response time of the comparator and its CMOS latch is crucial for the design of a high speed FLASH A/D converters. In the metastability study of a flip-flop [7], it is shown that the response time of positive feedback CMOS latch composed of 2 cross-coupled inverters is directly proportional to the time constant $\tau$ defined as:

$$\tau = C/g_m \qquad (2)$$

where $g_m$ is the transconductance of the inverter and C, the capacitance seen at the output. In order to reduce the response time of the CMOS latch, the transconductance of the inverter should be maximized. This is usually done by increasing the W/L ratio of the transistors. Increasing the ratio W/L also increases the capacitance C. It is then clear that a compromise has to be found in order to obtain the optimal $C/g_m$ ratio.
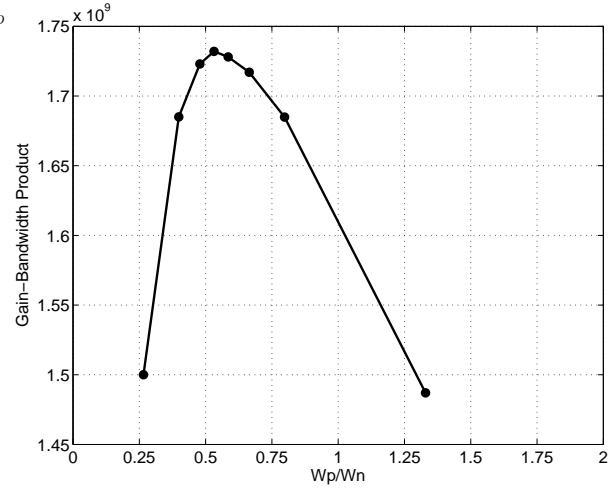
Using AC analysis, it has been shown, in [8], that the response time of a CMOS latch is directly proportional to the inverters gain bandwith product (GBW). By maximizing the GBW around the metastable voltage, $V_m$, the response-time is optimized. In figure 3, we show the GBW of the CMOS latch (Mn1, Mn2, Mp3, Mp4) in function of the ratio $W_p/W_n$. This curve was obtained using AC simulations of the CMOS latch while transistors M5 and M6 are biased for $I_0 = 20\mu A$. The length of both NMOS and PMOS transistors were fixed to minimum value ($L_n = L_p = L_{min} = 0.18\mu m$). Figure 3 shows that maximum GBW is obtained for a $W_p/W_n$ ratio approximately equal to 0.5.

## 4. The SR latch

The comparator output is latched by an SR latch. When the sampling frequency, $f_s$, is at $500MHz$, the difference between $V_{out+}$ and $V_{out-}$ is not high enough so that the SR latch takes the decision to store a logic '1' or a '0'.
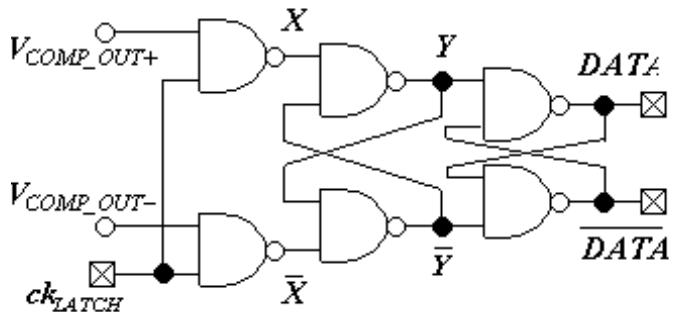


Figure 4. The positive feedback circuit amplifying the difference between $V_{out+}$ and $V_{out-}$ to digital '1' and '0' levels.
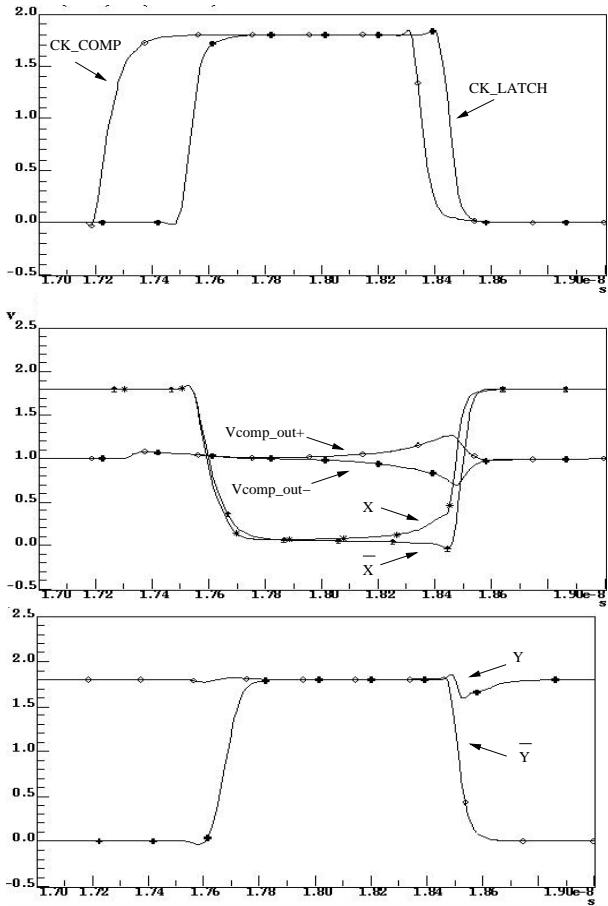
Figure 5. The signals of circuit described by figure 4.

In order to overcome this problem, and to increase the sensitivity of the latch, the circuit shown in Fig.4 is used. The output signals from the comparator $V_{out+}$ and $V_{out-}$ go through 2 NAND gates with the clock signal $CK_{LATCH}$. During the RESET phase, as soon as $CK_{LATCH}$ is high, the output signals of the NAND gates, $X$ and $\overline{X}$, fall to '0'. The latch, which is composed of 2 cross-coupled NAND gates, is then in an unstable state since both its ouputs $Y$ and $\overline{Y}$ become simultaneously equal to '1'. During the EVALUATION phase, as soon as the clock signal $CK_{LATCH}$ falls to '0', the outputs $Y$ and $\overline{Y}$ toggle to a stable state depending on the delay between the 2 inputs $X$ and $\overline{X}$ [9]. Note that mismatch errors between the 2 NAND gates, having $X$ and $\overline{X}$ as inputs and $Y$ and $\overline{Y}$ as ouputs, will have an important impact on the precision of the comparator.

The final digital results $DATA$ and $\overline{DATA}$ are obtained using 2 additional cross-coupled NAND gates. The detailed operation of this circuit is illustrated in figure 5.

## 5. Simulation Results

A 4-bit FLASH A/D converter has been designed using the architecture described in section 2 and the current comparator described in section 3. With a biasing current
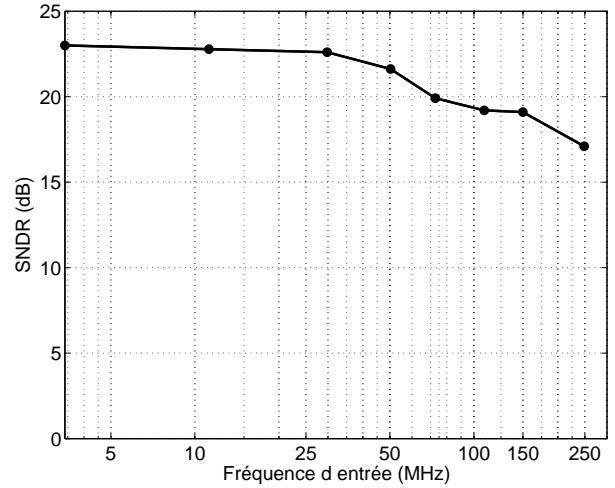


Figure 6. Signal to Noise and Distortion Ratio (SNDR) in function of the input frequency.

of $I_0 = 20\mu A$, the maximum input signal swing was fixed to $I_{in} = I_{ref} = \pm 15\mu A$.

The A/D converter was simulated with a sampling frequency of 500 MHz. In order to measure the Signal-to-Noise and Distortion Ratio (SNDR) of the converter, several simulations have been performed with different input signal frequency varying from a few MHz to 250 MHz. These input signals were applied using maximum input signal amplitude. A 1024 points FFT is then applied to the output signal to calculated the Signal-to-Noise and Distortion Ratio. The results of these simulations are illustrated in figure 6. The power consumption of the analog circuit is $3mW$.

## 6. Conclusion

In this paper, we have proposed to use a current-mode comparator to realize FLASH analog-to-digital converter. A design method based on the gain bandwidth product of the CMOS latch is used to optimize the sizing of the comparator transistors. Forcing the SR latch following the comparator to an unstable state during the EVALUATION phase significantly increases the sensitivity and the maximum sampling frequency of the A/D converter. Using these techniques, a 4-bit FLASH A/D converter sampling at 500 MHz has been designed and simulated in a $0.18\mu m$ CMOS process. Compared to other implementations, the power consumption of the proposed circuit is interesting.

# References

[1] T.N. Blalock and R.C. Jaeger. "A High-Speed Clamped Bit-Line Current-Mode Sense Amplifier". *IEEE Journal of Solid-State Circuits*, vol. 26(No. 4):542–548, April 1991.

[2] L.G. Roeintan and A.M. Sodagar. "High-speed current-mode sense amplifier". *Electronics Letters*, vol. 30(No. 17):1371–1372, 18th August 1994.

[3] S. Yoo, C. Kim, S. Jung, K. Baek, and S. Kang. "New Current-Mode Sense Amplifiers for High Density DRAM and PIM architecture". *IEEE International Symposium on Circuits And Systems.*, pages 938–941, May 2001.

[4] H. Aboushady, F. Montaudon, F. Paillardet, and M.M. Louërat. "A 5mW, 100kHz, Current-Mode Continuous-Time Sigma-Delta Modulator with 84dB Dynamic Range". *European Solid-State Circuits Conference, ESSCIRC*, September 2002.

[5] J.A. Bell, J.W. Bruce, B.J. Blalock, and P.A. Stubberd. "Current Mode Flash Analog-to-Digital Converter". *IEEE Midwest Symposium on Circuits And Systems.*, pages 272–275, August 2001.

[6] H. Aboushady and M.M. Louërat. "Low-Power Design of Low-Voltage Current-Mode Integrators for Continuous-Time $\Sigma\Delta$ Modulators". *IEEE International Symposium on Circuits And Systems.*, pages 276–279, May 2001.

[7] T. Kacprzack and A. Albicki. "Analysis of metastable operation in RS CMOS Flip Flop". *IEEE Journal of Solid-State Circuits*, vol. 22(No. 1):57–64, February 1987.

[8] L.Kim and R.W Dutton. "Metastability of CMOS Latch/Flip-Flop". *IEEE Journal of Solid-State Circuits*, vol. 25(No. 8):942–951, August 1990.

[9] A.S. Sedra and K.C. Smith. *"Microelectronic Circuits"*. Saunders College Publishing, 1991.