Sinusoidal RF DACs for Undersampled LC Bandpass $\Sigma\Delta$ Modulators

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***Abstract*— In this paper, we present a systematic technique to design bandpass LC $\Sigma\Delta$ modulators with sinusoidal feedback DACs. The output resistance of the DAC degrades the quality factor of the LC resonator and the DAC output capacitance modifies its resonance frequency. It is shown that the DAC output resistance should be taken into account while designing the Q enhancement circuit of the integrated LC resonator. The resonance frequency is adjusted by modifiying the parallel capacitor of the LC resonator. Using the proposed method, different sinusoidal 3.256 GHz DACs are designed in a CMOS 0.13μm process. Simulation results are presented to compare their performances in the context of an undersampled LC $\Sigma\Delta$ modulator.**

I. Introduction

Recent years have shown an increasing interest to digitize the input signal near the front end of RF receivers so as to push more signal processing functions into the digital domain. LC filter based $\Sigma\Delta$ modulators, shown in Fig. 1, have been considered for direct digitization at RF frequencies [1]–[3].
At high sampling frequencies, the use of sinusoidal feedback DAC signals has been proposed to reduce Signal-to-Noise Ratio degradation due to clock jitter [4]–[7]. Furthermore, if the undersampling technique is used, it is necessary to upconvert the feedback signal to the modulator's center frequency by mixing it with a sinewave [8]–[10]. Systematic design methods for the system level design of bandpass LC $\Sigma\Delta$ modulators using sinusoidal feedback signals has been presented in [10], [11].
Integrated LC resonators have a low quality factor and a Q-enhancement circuit is usually needed to increase their quality factor to a reasonable value. In an LC $\Sigma\Delta$ modulator, the DAC output is connected to the LC resonator. As illustrated in Fig.**??**, the DAC output resistance can have a significant effect on the resonator's quality factor, Q, and the DAC output capacitance can alter the center frequency, f_0, of the resonator.
In this paper we focus on the circuit level design of sinusoidal DACs. We present 3 different sinusoidal DAC structures: simple DAC, cascoded DAC and RDAC. We calculate and compare the output resistance of each structure. It is shown how to take the output resistance into account in the design of the Q-enhancement circuit.
The output capacitances of the different DAC structures are also calculated and taken into account in the design of the resonator.

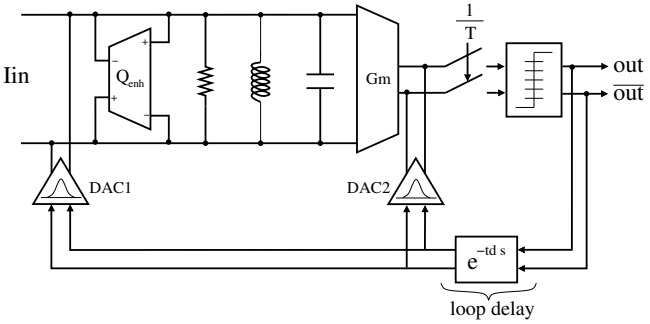

Fig. 1. 2^{nd} order LC bandpass $\Sigma\Delta$ modulator.

II. Different Sinusoidal DAC structures

In this section, we present 3 different structures to realize a differential sinusoidal current output DAC. These DACs are based on the same principle. They all have a positive sinusoidal current source and a negative sinusoidal current source. Depending on the DATA fedback in the $\Sigma\Delta$ loop, these sinusoidal current sources are connected either to the positive or to the negative DAC output.

A. Simple DAC

the *simple dac* is illustrated in fig.2. the positive sinusoidal current source is realized using the biasing voltage, v_{bp}, the sinusoidal voltage source, v_{sp}, and the pmos transistor m6, biased in the saturation region. the negative sinusoidal current source is realized using the biasing voltage, v_{bn}, the sinusoidal voltage source, v_{sn}, and the pmos transistor m1, biased in the saturation region. transistors m2 and m3 are nmos switches, m4 and m5 are pmos switches. all these switches are biased in the linear region and are controlled by the $\sigma\delta$ digital feedback signals.
in order to function at a sampling frequency of 3.256 ghz, the digital feedback circuitry is realized using source coupled logic (scl). the output of scl circuits is limited between v_{dd} and $\frac{v_{dd}}{2}$. these outputs are directly applied to the nmos switches m2 and m3. for proper operation of the pmos switches, m4 and m5, scl output levels are shifted, to $\frac{v_{dd}}{2}$ and v_{ss}.
besides garantying a proper on-off operation of the switches, scl digital output signals have a high crossing point and shifted scl digital output signals have a low crossing point. these

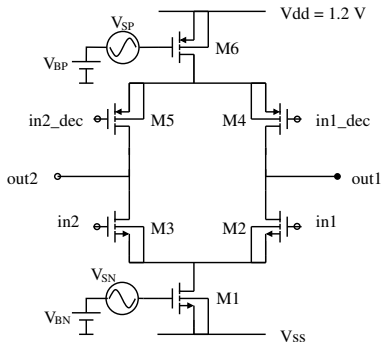

Fig. 2. simple dac.

signals can help reduce glitches that occur during switching since they ensure that the current from the current sources can always flow to either one of the outputs. in order to study the effect of connecting the dac to an integrated lc filter, we need to develop expressions for the output resistance and the output capacitance of the dac.

the output resistance of the *simple dac*, shown in fig.2, can be described by the following expressions:

$$\begin{aligned} r_{simple_n} &= (1+g_{m_2}r_{ds_2})r_{ds_1} + r_{ds_2} \\ r_{simple_P} &= (1+g_{m_5}r_{ds_5})r_{ds_6} + r_{ds_5} \end{aligned} \quad (1)$$

where R_{simple_N} is the resistance seen when the NMOS current source is connected to the output node through the NMOS switch and R_{simple_P} is the resistance seen when the PMOS current source is connected to the output node through the PMOS switch.

The output capacitance of the *Simple DAC* can be described by the following expressions:

$$\begin{aligned} C_{simple_N} &= c_{ds_2} + c_{db_2} + c_{dg_2} + c_{ds_4} + c_{db_4} + c_{dg_4} \\ C_{simple_P} &= c_{ds_5} + c_{db_5} + c_{dg_5} + c_{ds_3} + c_{db_3} + c_{dg_3} \end{aligned} \quad (2)$$

where C_{simple_N} is the resistance seen when the NMOS current source is connected to the output node through the NMOS switch and C_{simple_P} is the resistance seen when the PMOS current source is connected to the output node through the PMOS switch.

B. Cascoded DAC

The operation of the *Cascoded DAC*, shown in Fig.4, is similar to the *Simple DAC*. Cascode transistors are added above the NMOS et PMOS switches to increase the DAC output resistance, which can be described by the following expressions:

$$\begin{aligned} R_{cas_N} &= (1+g_{m_{2c}}r_{ds_{2c}})R_{simple_N} + r_{ds_{2c}} \\ R_{cas_P} &= (1+g_{m_{5c}}r_{ds_{5c}})R_{simple_P} + r_{ds_{5c}} \end{aligned} \quad (3)$$

From equation (3), we can see that the output resistance of the *Cascoded DAC* is approximately $g_{m_{2c}}r_{ds_{2c}}$ times higher than the output resistance of the *Simple DAC*.

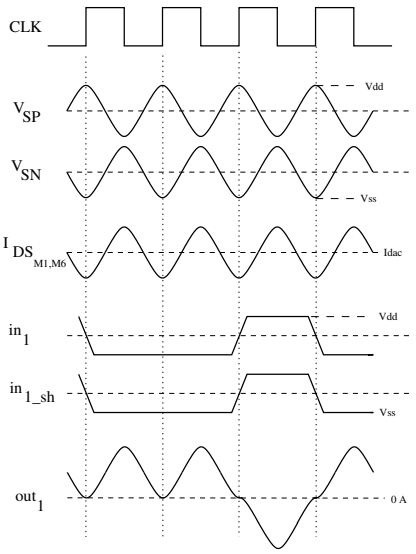

Fig. 3. Sinusoidal DACs principle.

The output capacitance of the *Cascoded DAC* can be described by the following expressions:

$$\begin{aligned} C_{cas_P} &= c_{ds_{5c}} + c_{db_{5c}} + c_{dg_{5c}} + c_{ds_{3c}} + c_{db_{3c}} + c_{dg_{3c}} \\ C_{cas_N} &= c_{ds_{2c}} + c_{db_{2c}} + c_{dg_{2c}} + c_{ds_{4c}} + c_{db_{4c}} + c_{dg_{4c}} \end{aligned} \quad (4)$$

Since transistors M2c-M5c are biased in the saturation region, it is expected that the output capacitance of the *Cascoded DAC* to be different from that of the *Simple DAC*.

Another advantage of cascoding the switches is to prevent voltage variations at the output node from reaching the drain of the current source transistor [12].

The main disadvantage of this structure is that it is difficult, when operating at low supply voltage, to ensure that the current source transistors and the cascode transistors are biased in the saturation region. Furthermore, high V_{TH} transistors are used for the switches so that the low level of the SCL digital output $\frac{V_{dd}}{2}$ would be sufficiently low to turn the switches OFF.

C. RDAC

In the *RDAC*, shown in Fig.5, the current source transistors are replaced by a resistance [13]. In this case, the output resistance can be described by the following expressions:

$$\begin{aligned} R_{rdac_N} &= (1+g_{m_2}r_{ds_2})R_1 + r_{ds_2} \\ R_{rdac_P} &= (1+g_{m_5}r_{ds_5})R_6 + r_{ds_5} \end{aligned} \quad (5)$$

The output capacitance is similar to that of the *Simple DAC*.

III. Quality Factor and Center Frequency Adjustement

A. Quality Factor, Q

Neglecting losses due to capacitors', integrated LC resonator's losses can be modeled by a series resistance, R_s, such that :

$$R_s = \frac{w_0 L}{Q_i} \quad (6)$$

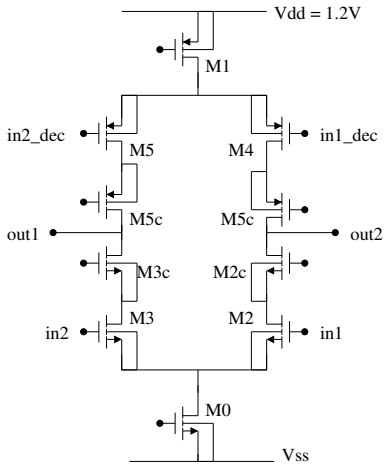

Fig. 4. Cascoded DAC.

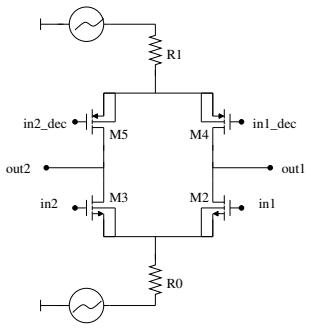

Fig. 5. RDAC.

where $w_0 = 2\pi f_0$ is the resonance frequency, L the value of the inductor and Q_i the intrinsic quality factor of the LC resonator at w_0. It is usually more convenient to express the resonator's losses near the resonance frequency by a parallel resistor, R_p, such that :

$$R_p = (1 + Q^2)R_s \approx Q_i w_0 L \tag{7}$$

Integrated LC resonators have a low quality factor and a Q-enhancement circuit is usually needed to increase their quality factor to a reasonable value. The Q-enhancement circuit is usually an active negative resistance, $R_{-ve} = \frac{1}{G_m}$, which reduces the overall resonator's losses in order to achieve the desired quality factor, Q_d.
In an LC $\Sigma\Delta$ modulator, the DAC's output resistance, R_{out}, is, as shown in Fig.6, connected in parallel with the LC resonator. In this case, the Q-enhancement circuit has to take into account the losses introduced by R_{out} such that:

$$\begin{aligned} R_{p_{eq}} &= R_p // R_{out} // R_{-ve} \\ \frac{1}{R_{p_{eq}}} &= \frac{1}{R_p} + \frac{1}{R_{out}} + \frac{1}{R_{-ve}} \end{aligned} \tag{8}$$

From equations 7 and 8, we can find an expression for the required negative resistance R_{-ve} in order to achieve the desired quality factor, Q_d,

$$\frac{1}{R_{-ve}} = \frac{1}{Q_d w_0 L} - \left(\frac{1}{R_p} + \frac{1}{R_{out}}\right) \tag{9}$$

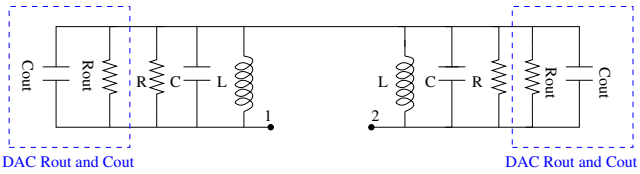

Fig. 6. Model of the differential LC resonator connected to the feedback DAC. The losses of the Q-enhanced resonator are modeled by the parallel resistor $R_{Q_{enh}}$.

Equation 9 permits us to have an expression for the transconductance of the Q-enhancement circuit:

$$G_m = \frac{1}{w_0 L}\left(\frac{1}{Q_d} - \frac{1}{Q_i}\right) - \frac{1}{R_{out}} \tag{10}$$

B. Center Frequency, f_0

The resonance frequency of an LC resonator is defined by the following relation:

$$w_0 = \sqrt{\frac{1}{LC}} \tag{11}$$

In the context of an LC $\Sigma\delta$ modulator the equivalent parallel capacitor is equal to

$$C_{p_{eq}} = C_p + C_{out} + C_{-ve} \tag{12}$$

where C_{out} is the DAC output capacitance and C_{-ve} is the parasitic capacitance due to the Q-enhancement circuit.
In order to have a resonance frequency equal to w_0, we should adjust the value of the parallel capacitor C_p so that:

$$C_p = \frac{1}{{w_0}^2 L} - C_{out} - C_{-ve} \tag{13}$$

IV. Design Examples & Simulation Results

We consider a 2^{nd} order undersampled LC bandpass $\Sigma\Delta$ modulator as shown figure 1. The undersampling factor M is $\frac{2}{3}$ [10] since the input signal is 2.442GHz and the sampling frequency is 3.256GHz and the loop delay is one sampling period and a half. The different architectures of sinusoidal DACs implemented in transistors are placed in the modulator and the LC filter is adapted for each DAC to compensate their output impedance derived in table IV. The figure 8 validates this method by showing that the different DACs architectures achieve the same results as an ideal DAC.

V. Conclusion

In this paper, we have derived relations to calculate the transconductance of the Q enhancement circuit in function of the desired Quality factor for the resonator, the intrinsic Quality factor of the resonator and the output resistance of the $\Sigma\Delta$ feedback DAC. We have also derived some relations to calculate the resonators capacitance in function of the desired resonance frequency and the output capacitance of the $\Sigma\Delta$ feedback DAC. We have successfully used these equations to design the Q enhancement circuit and the capacitor of

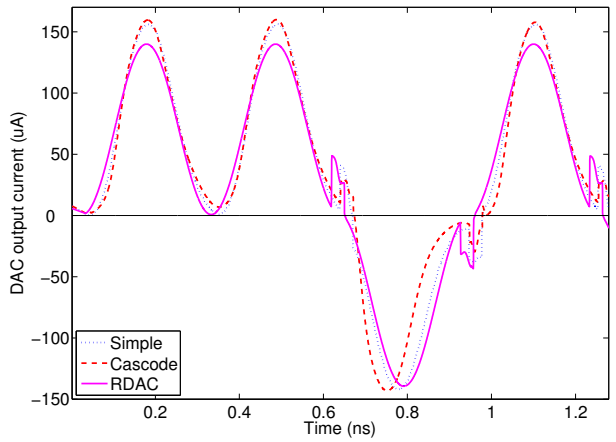

Fig. 7. Sinusoidal DACs output current.

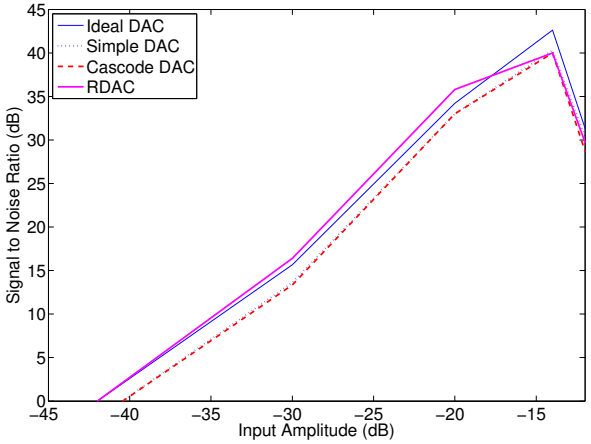

Fig. 8. Simulated 2nd order undersampled LC bandpass $\Sigma\Delta$ with different feedback DACs.

the LC resonator for different $\Sigma\Delta$ feedback DAC structures. Transistor level simulations of undersampled LC bandpass Sigma-Delta modulators operating at a center frequency of 2.442 GHz and a sampling frequency of 3.256 GHz, were used to validate the proposed method.

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TABLE I

LC FILTER ADJUSTMENTS TO COMPENSATE THE DACS OUTPUT IMPEDANCE.

DACs	Rout	R	Gm
Ideal DAC	∞	6.18 kΩ	-1.4664 m℧
Simple DAC	87.8 kΩ	6.64 kΩ	-1.4778 m℧
Cascoded DAC	431.75 kΩ	6.27 kΩ	-1.4687 m℧
RDAC	10.98 kΩ	14.12 kΩ	-1.5575 m℧

	Cout	Cp
Ideal DAC	0	1.0552 pF
Simple DAC	2.3965 fF	1.0528 pF
Cascoded DAC	7.2586 fF	1.0476 pF
RDAC	2.3965 fF	1.0528 pF