Continuous-Time $\Sigma\Delta$ Modulators With VCO-Based Voltage-to-Phase and Voltage-to-Frequency Quantizers

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***Abstract*— In this paper, two different VCO-Based quantizers architectures are implemented and compared as multi-bit quantizers of Continuous-Time (CT) Sigma-Delta ($\Sigma\Delta$) modulator. The first one is the voltage-to-frequency while the second is the voltage-to-phase architecture. Two 4^{th} order CT-$\Sigma\Delta$ modulators are designed with Voltage-to-frequency and voltage-to-phase quantizers respectively. Both modulators are designed and simulated in 0.13μm technology. The comparision shows that voltage-to-phase quantizer remarkably reduces the VCO non-linearity and increases the modulator's maximum SNR .**

I. Introduction

Modern wireless communication systems require high performance A/D converters with increasing bandwidth and resolution. Sigma-Delta modulators are usually used for high resolution while the use of multi-bit quantizers is necessary to maintain the high-resolution at wide-band operation [1] [2].

A Continuous-Time (CT) Sigma-Delta ($\Sigma\Delta$) modulator with a VCO-based time-domain quantizer is shown in Fig. 1. VCO-based quantizers, such as voltage-to-frequency [3] and voltage-to-phase [4], emerge as potential candidates for modern CMOS technology due to the fact that they are less sensitive to supply voltage reduction compared to conventional voltage quantizers.

The use of a voltage-to-frequency quantizer [3] [4] as a multi-bit quantizer inside the loop of a CT $\Sigma\Delta$ modulator reduces the total power consumption as well as the VCO non-idealities. This architecture is characterized by the abscence of power-hungry comparators, inherent Data Weighted Averaging (DWA) and additional noise shaping properties. The drawback of voltage-to-frequency quantizers is the limited input signal range due to VCO non-linearity.

In a previous work, a systematic method was proposed to calculate the coefficients of a CT $\Sigma\Delta$ modulator with VCO-based voltage-to-frequency quantizer considering loop delay compensation [5]. This technique is based on the discrete-time to continuous-time (DT-CT) equivalence [6].

In this work, CT $\Sigma\Delta$ modulators with voltage-to-frequency and Voltage-to-phase quantizers are designed and compared. Both CT $\Sigma\Delta$ modulators have the same performance of a DT $\Sigma\Delta$ of the same order. System-level optimization allowed to relax the specifications of the opamps used in the circut implementation.

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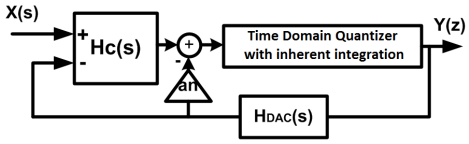

Fig. 1. Continuous-Time $\Sigma\Delta$ modulator with VCO-based time-domain quantizer.

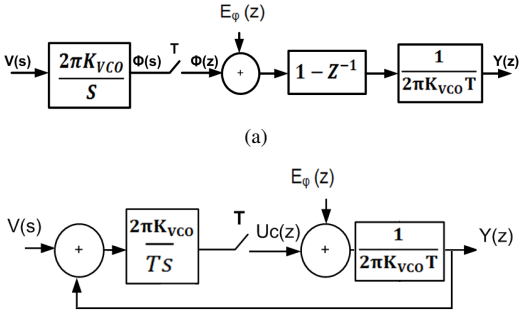

Fig. 2. (a) Linear model of a voltage-to-frequency quantizer (b) Linear model of voltage-to-phase quantizer

In section II, the theory of operation of both quantizers architectures is illustrated. Section III presents the design method for discrete-time to continous-time transformation considering the quantizer architecture and the loop delay compensation. In section IV, design examples are presented and system level and transistor level simulation results are shown for wide-band specifications. The conclusion is presented in section V.

II. Voltage-to-Frequency And Voltage-to-Phase Architectures

The linear model describing the architecture of the voltage-to-frequency quantizer is shown by Fig. 2(a). A CT integrator with gain $2\pi K_{vco}$ represents the VCO. The VCO output phase is sampled at the integrator output and a discrete time differentiator converts the phase to frequency. The quantization noise is first order shaped by the differentiator. Dividing by $2\pi K_{vco}T$ converts the output frequency f_{vco} to voltage in

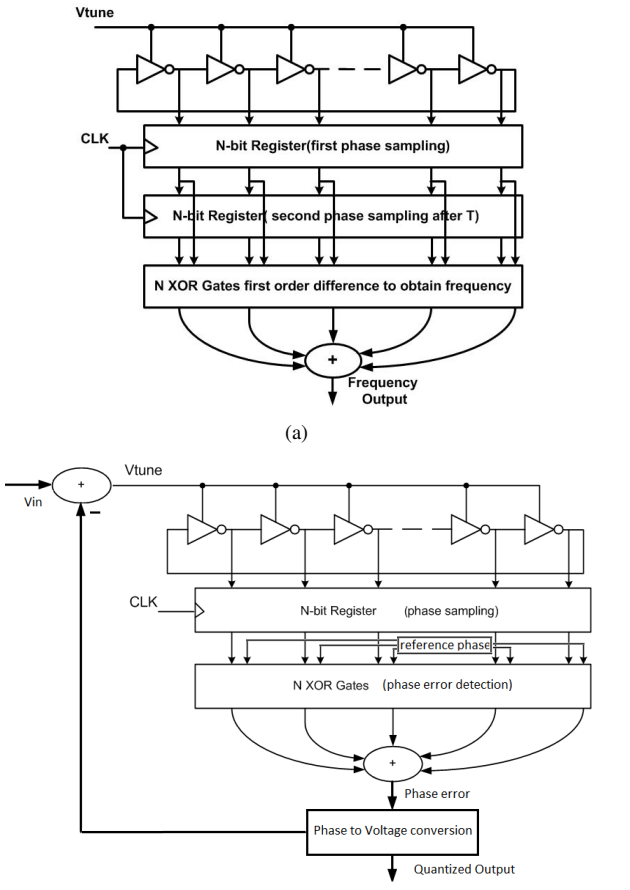

Fig. 3. VCO-based quantizer implementations (a) Voltage-to-frequency (b) Voltage-to-phase .

order to feed the $\Sigma\Delta$ modulator DACs without changing the modulator NTF.

Fig. 2(b) depicts the linear model of the voltage-to-phase quantizer that is similar to the VCO-based quantizer except that the output in this case is the phase instead of frequency and it is substracted from the input after being converted to voltage. The model is similar to that of a $\Sigma\Delta$ modulator of the first order and hence have an inherent first order noise shaping property. Quantizers implementation is shown in Fig. 3. A multi-phase Ring VCO where the inverters delay is set by the control voltage is the main block in both implementations. For the voltage-to-frequency quantizer, the VCO outputs are sampled and compared with the previous sample resulting in a first order difference. For voltage-to-phase quantizer, the multi-phase output of the VCO is compared to a multi-phase reference and the phase error is converted to voltage and substracted from the input.

The main idea in the voltage-to-phase quantizer is that the control voltage of the Ring VCO is only the error between the quantized output and the quantizer input. This way, the VCO characteristics may be assumed linear and the VCO keeps oscillating near its free-running frequency.

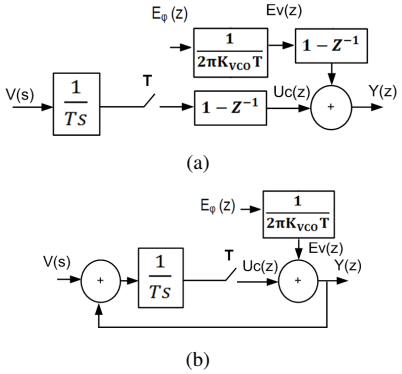

Fig. 4. Linear Model with quantization noise converted from phase to Voltage (a) voltage-to-frequency quantizer (b) voltage-to-phase quantizer.

The reference multi-phase generated is dependant on the free-running frequency and the number of the VCO stages. For N-bit Ring VCO, there are $2 * (2^N - 1)$ possible output phase states while for a free-running frequency as $\frac{f_s}{4}$, four reference phases are needed.

Yet to note that voltage-to-phase quantizer misses the barrel-shift property of the voltage-to-frequency quantizer [3] and according to the target specifications the modulator may need a dedicated DWA circuit to drive the DACs [4] or a careful matched layout for the DAC current cells [2].

III. Design of CT $\Sigma\Delta$ with VCO-Based Time Domain Quantizers

A. DT-to-CT Transformation For CT $\Sigma\Delta$ With VCO-Based Time Domain Quantizers

The discrete-time to continuous-time transformation [6] determines the coefficients of an N^{th} order CT $\Sigma\Delta$ modulator with the same Noise-Transfer-Function (NTF) of a DT $\Sigma\Delta$ modulator of the same order. For a DT $\Sigma\Delta$ modulator of a general order N, the corresponding $NTF_d(z)$ is

$$NTF_d(z) = \frac{1}{1 - G_d(z)} \tag{1}$$

The model of Fig.2 has to be rearranged to allow determining $NTF_c(z)$ with quantization noise represented in terms of voltage instead of phase. Then the $NTF_c(z)$ can be found combining the linear models of Fig. 1 and Fig. 4

$$NTF_c(z) = \frac{Y(z)}{E_v(z)} = \frac{1}{1 - G_c'(z)} \tag{2}$$

For a $\Sigma\Delta$ modulator with voltage-to-frequency quantizer $G_c^{'}(z)$ is

$$G_{c,vfr}^{'}(z) = -\frac{z^{-1}}{1 - z^{-1}} - \mathcal{Z}\left\{H_{DAC}(s)(\frac{a_n}{Ts} + \frac{H_c(s)}{Ts})\right\} \tag{3}$$

While for an voltage-to-phase quantizer $G_c^{'}(z)$ is

$$G_{c,vph}^{'}(z) = -\mathcal{Z}\left\{H_{DAC}(s)(\frac{a_n}{Ts} + \frac{H_c(s)}{Ts})\right\} \tag{4}$$

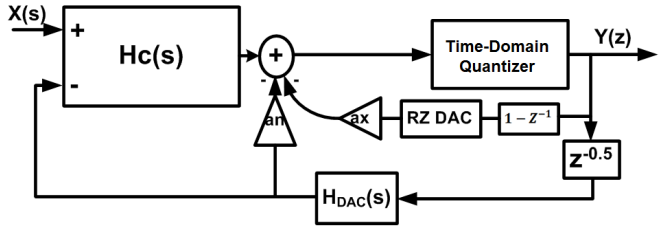

Fig. 5. CT ΣΔ modulator with VCO-based quantizer and loop delay compensation.

where T is the sampling period, $H_{DAC}(s)$ is the feedback DAC transfer function, $H_c(s)$ is the loop filter transfer function and a_n is the additional feedback coefficient which compensates the inherent integration of the VCO-based quantizers. Through symbolic equivalence between $G_c^{'}(z)$ of (2) and $G_d(z)$ of (1), the coefficients of similar z orders are equated and the CT ΣΔ modulator coefficients are determined

B. Loop-Delay Compensation

The traditional loop-delay compensation technique [7] can not be applied directly on CT ΣΔ modulators with VCO-based quantizers as shown in [5] due to the in herent integration of the quantizers. The same solution of [5] is used for both quantizer architectures as shown in Fig. 5. A discrete time differentiator is added in this branch in order to cancel the inevitable integration seen in this path. The use of a RZ DAC in this branch allows to mask the circuit delay without altering the modulator's NTF. This method should allow masking delays within $0.5T$ and the corresponding new loop gain $G_c^{''}(z)$ is given by (5) and (6) for modulators with voltage-to-frequency and voltage-to-phase quantizers respectively.

$$G_{c,vfr}^{''}(z) = -\frac{z^{-1}}{1-z^{-1}} - z^{-0.5}\mathcal{Z}\left\{H_{DAC}(s)\left(\frac{a_n}{Ts} + \frac{H_c(s)}{Ts}\right)\right\} - (1-z^{-1})\mathcal{Z}\left\{H_{RZ\,DAC}(s)\frac{a_x}{Ts}\right\} \quad (5)$$

$$G_{c,vph}^{''}(z) = -z^{-0.5}\mathcal{Z}\left\{H_{DAC}(s)\left(\frac{a_n}{Ts} + \frac{H_c(s)}{Ts}\right)\right\} - \mathcal{Z}\left\{H_{RZ\,DAC}(s)\frac{a_x}{Ts}\right\} \quad (6)$$

Where $H_{RZ\,DAC}(s)$ is the RZ DAC transfer function and a_x is the added coefficient for compensating loop delay. Symbolic equivalence is made between the new loop gain $G_c^{''}(z)$ and $G_d(z)$ of (1) to find the exact coefficients of a CT ΣΔ modulator with first order noise shaping time domain quantizer of a general order while considering loop delay compensation.

IV. Simulation Results

A. Design Example For CT ΣΔ Modulator With Voltage-to-Phase and Voltage-to-Frequency Quantizers

A 4^{th} order DT ΣΔ modulator with 4-bit quantizer is designed using Schreier Delta-Sigma toolbox [8] for the following wide-band specifications: OSR=16, bandwidth=20 MHz and f_s=640 MHz. The design method presented in section III is used to get the equivalent CT ΣΔ modulator coefficients for each of the time-domain quantizers considering the loop delay compensation. Fig. 6(a) shows the 4th order DT ΣΔ modulator linear model using a Cascade of Integrators in Feedforward (CIFF) architecture. The CT ΣΔ modulator equivalent model with voltage-to-frequency quantizer and voltage-to-phase quantizer are shown in Fig. 6(b) and Fig. 6(c) respectively.

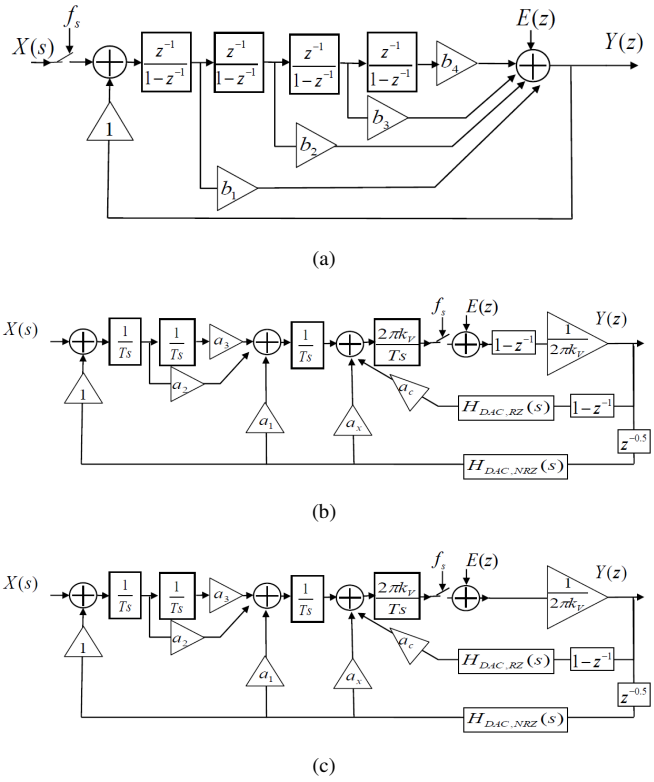

Fig. 6. 4^{th} order ΣΔ modulator CIFF (a) DT (b) CT with voltage-to-frequency quantizer (c) CT with voltage-to-phase quantizer

The output power spectral density of the CT ΣΔ modulator with both VCO-based quantizers is equivalent to that of the DT ΣΔ modulator as shown in Fig. 7. The results ensure that the CT ΣΔ modulators with different time-domain quantizers designed with the DT-to-CT transformation achieve a performance identical to the DT ΣΔ modulator of the same order.

B. Transistor Level Simulation and VCO Non-linearity

Two CT-ΣΔ modulators are designed and realized in transistor level using 0.13 μm CMOS technology, one with voltage-to-frequency quantizer and the second with voltage-to-phase quantizer. The DACs are ideally modeled and the circuit used is shown in Fig. 8. The parallel branches of Fig. 6 are gathered in a single block for simplification. Through system level design, the opamp specifications are relaxed and a single stage opamp with 30 dB DC gain and 800 MHz unity gain frequency was adequate for an acceptable performance. The opamp circuit topology and the ring-VCO cell are shown in Fig. 9(a) and Fig. 9(b) respectively The output power

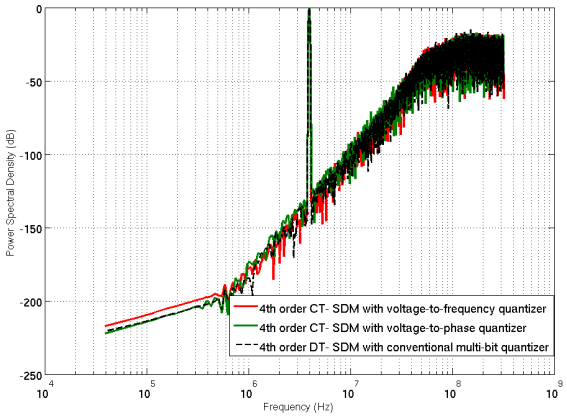

Fig. 7. The output Power Spectral Density for DT $\Sigma\Delta$ modulator and ideal CT $\Sigma\Delta$ modulator with voltage-to-frequency quantizer and voltage-to-phase quantizer considering loop-delay compensation

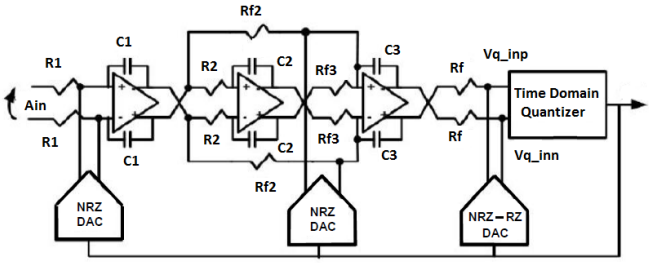

Fig. 8. Designed circuit of a 4th order CT $\Sigma\Delta$ modulator with VCO-based quantizer and loop-delay compensation

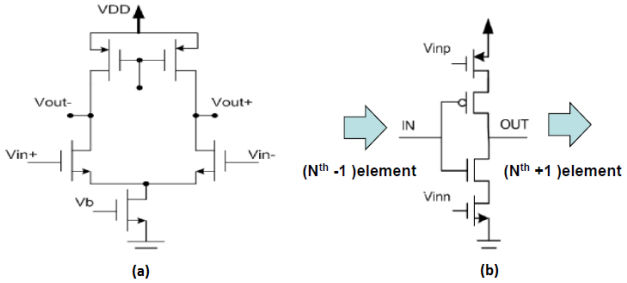

Fig. 9. (a) Single stage opamp circuit (b)Ring-VCO unit cell

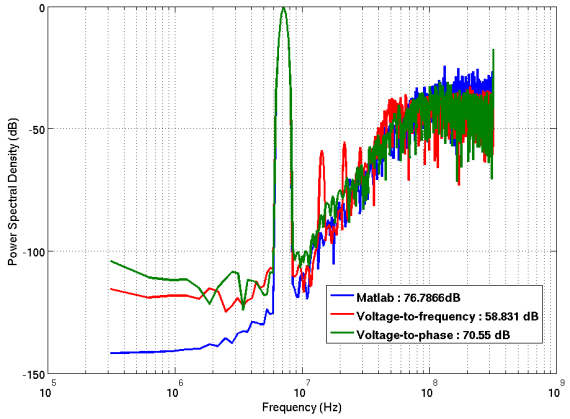

Fig. 10. Output power spectral density of a transistor level simulation of a 4^{th} order CT $\Sigma\Delta$ modulator with voltage-to-frequency quantizer compared to voltage-to-phase quantizer with only the DACs idealy modeled.

spectral density (PSD) from transistor level simulations of both modulators is shown in Fig. 10 compared to the ideal modulator PSD with -10 dB input signal.

A harmonic distortion appears in the output spectrum of the modulator with voltage-to-frequency quantizer degrading the SNR to 58.8 dB while no significant harmonic components exist with the use of voltage-to-phase quantizer where its SNR achieves 70.5 dB.

V. Conclusion

In this paper, we presented and compared two VCO-based quantizers as multi-bit quantizers for CT $\Sigma\Delta$ modulators. The Voltage-to-phase quantizer misses the inherent DWA property of the voltage-to-frequency quantizer but is less sensitive to VCO non-linearity. CT-DT transformation is used to design a general order CT $\Sigma\Delta$ modulator for each quantizer. Two 4^{th} order CT $\Sigma\Delta$ modulators with 4-bit quantizer are designed in 0.13 μm CMOS technology. The first uses a voltage-to-frequency quantizer while the second uses a voltage-to-phase quantizer. The comparision shows that the modulator using voltage-to-phase quantizer remarkably reduces the VCO non-linearity and increases the modulator maximum SNR.

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