LNA Automatic Synthesis and Characterization for Accurate RF System-Level Simulation

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***Abstract*— In this paper, we propose an automatic design procedure for the synthesis of a cascode LNA with inductive source degeneration. The proposed method is based on the precise characterization of noise figure, input impedance and gain. The design procedure is implemented in a C++ environment using a BSIM3v3-based tool for transistor sizing and a symbolic computation tool for circuit characterization. SystemC AMS can then be used to perform a system level simulation of a complete RF receiver using precise model of the LNA. Considering the complete equivalent model for the transistors and the inductors, two LNAs operating at 2.4 GHz and 935 MHz are synthesized and characterized for a 130 nm CMOS process. The generated accurate model is then used in a high-level simulation of a complete QPSK-based RF receiver to study the effect of the LNA noise figure on the Bit Error Rate of the receiver.**

I. Introduction

In recent years, the main effort of RF circuit designers is concentrated on responding to the higher demand for smaller, lighter, cheaper, and of higher performance wireless devices. To help RF designers reach these goals, automatic design procedures for some RF blocks have been proposed [1] [2]. Having a systematic design results in a general and fast solution which can be applied for different specifications and topologies. To design and characterize an RF receiver chain (Fig. 1), as the first step we need to determine the specifications of each block, secondly the circuit design of blocks is made to satisfy these specifications and at last the characterization can be done.

System simulation, the first step in an RF receiver design, is done in Matlab or ADS and consists of the manipulations to adjust the specifications of each block such as noise figure (NF), gain and third-order intercept point (IP3). After the circuit design the simulation tools as ELDO-RF characterize the blocks.

RF circuit design is a relativly complex procedure involving several design constraints and trade-offs between the parameters, such as noise figure (NF), gain, power consumption and input impedance [3], that leads us to implement an automatic procedure which takes the majority of these contraints into account. The optimization procedures are usually applied by several researchers most of which are based on simulation methods that demand several iterations between the design system and the simulator which ends in an important execution time [4] [5]. To avoid these iterations, we can use the approximate equations of parameters or apply an automatic

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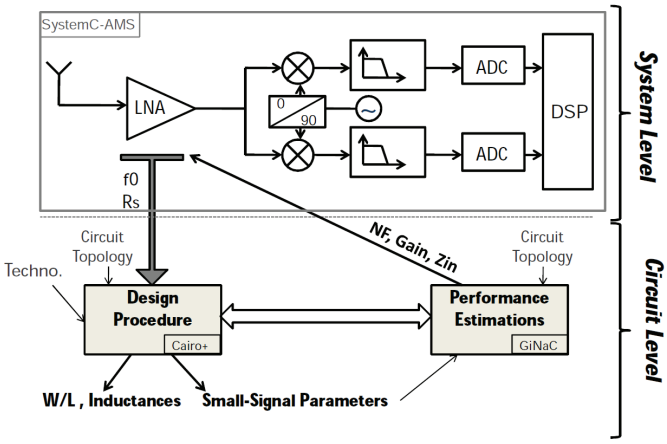


Fig. 1. The proposed C++ based environment for the automatic design and characterization of RF transceivers. (Simulation → SystemC AMS, Synthesis → CAIRO+, Characterization → GiNaC)

system to find the exact value of each parameter considering the equivalent model of all components [1].

In this paper, we propose an automatic procedure to implement three phases of the receiver chain design in the same environment (C++). The system level simulation is implemented in SystemC AMS [6] and the circuit design and characterization in CAIRO+ [7] and GiNaC [8] respectively.

In section II, we give a brief introduction to LNA systematic design and characterization. In section III, the proposed approach of design and characterization is presented. In section IV, this technique is applied to two design examples and their simulation results are discussed. The conclusion is given in section V.

II. LNA systematic design and characterization

The cascode LNA with inductive source degeneration topology (Fig. 2) [9] has been synthesized. The most important feature of the cascode transistor is that a common-gate stage results in a higher power gain compared to a single stage. The degeneration technique has several advantages over the other matching techniques. It is simple and requires only one supplementary series component. A current-mirror concept is applied to bias the transistor M1. The load inductance is used to control the gain.

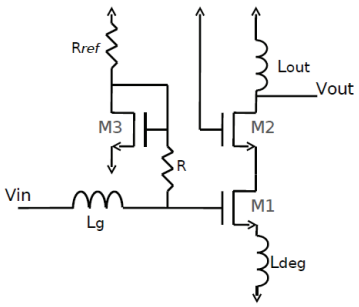


Fig. 2. The targeted circuit topology: cascode LNA with inductive source degeneration.

A. DC Biasing

Biasing the transistors, we need to decide about the gate voltage V_{gs} and the drain voltage V_{ds}. For this architecture V_{ds} and V_{gs} of all the transistors is chosen to be $\frac{V_{dd}}{2}$. This value is chosen because it will allow to have the same size of M1 and M2. Thus we also design the biasing circuit to have the V_{gs} equal to $\frac{V_{dd}}{2}$.

B. Transistors Sizing

The length of the transistor is chosen as the minimum size. It will give the best frequency performance of the transistor due to minimum parasitic capacitances. The width of the transistor is directly defined by the choice of current. The noise figure evolution by varying the bias current (Fig. 3) implies that there is a drain current that ends in minimum noise figure. We consider this behaviour to choose the transistor width and achieve the minimum noise figure.

C. NF characterization

The noise modeling of the RF transistor is presented in Fig. 4. The classic long channel noise theory for intrinsic MOS transistors defines two noise sources that are present at the device terminals. The first is the drain noise current which originates from the conductance of the channel, and the second is the induced gate noise current which originates from the charge fluctuations in the channel when the drain current fluctuates. An integrated inductor presents some parasitics resistances and capacitances. Resistances are due to intrinsic resistance of the employed metal, interconnections, skin effect

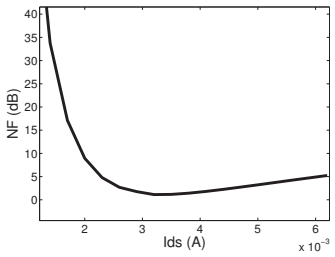


Fig. 3. The variation of the LNA Noise Figure in function of its biasing current. The Noise Figure is calculated using CAIRO+ and GiNaC for a 130nm CMOS process.(V_{ds}=V_{gs}=0.6 V)

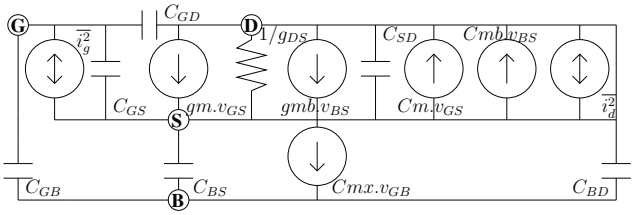


Fig. 4. The complete small signal MOS transistor model [12] (where: C_m= C_{dg}-C_{gd}, C_{mb}= C_{db}-C_{bd} and C_{mx}= C_{bg}-C_{gb}), used in the proposed automatic synthesis and characterization procedure.

at high frequencies and lossy substrate. The inductor with these parasitics can be modeled using the π-model [10].
The noise factor can be expressed as [11]:

$$F = 1 + \frac{N_{o(added)}}{N_{o(source)}} \tag{1}$$

where $N_{o(added)}$ is the added noise at output and $N_{o(source)}$ is the noise at the output originating at the source.

Using (1), the characterization of noise factor would require to know all the noise sources which are produced by the circuit components multiplied by the transfer function of each to obtain the additional noise at the output. In result we have:

$$F = f(\overline{i_d^2}|H_d|, \overline{i_g^2}|H_g|, \overline{i_R^2}|H_R|, \overline{i_{Rsub}^2}|H_{Rsub}|, \overline{i_{Rs}^2}|H_{Rs}|, G.N_i) \tag{2}$$

Where $\overline{i^2}$ and $|H|$ are the value of modeled noise source and the transfer function magnitude of each component, G and N_i are the power gain and input noise respectively.

D. Choice of inductors

The degeneration method requires two inductors to provide the power and noise match for the LNA. Besides, by adding the inductor at the source we can achieve unconditional stability [13]. The input impedance for this transistor (assuming that r_0 is not significant at the frequency of interest) is approximativly presented by (3).

$$Z_{in}(s) = \frac{1}{sC_{gs}} + s(L_{deg} + L_g) + \frac{g_m}{C_{gs}}L_{deg} \tag{3}$$

Where L_{deg}, L_g and C_{gs} are the degeneration inductor, the gate inductor and the gate-source capacitor respectively (Fig. 2). Note that to be matched, the real part of the input impedance must be equal to the source resistance R_s. To obtain a real impedance at the input, the capacitive part of impedance should be compensated with inductances [9]. As mentioned above, these decisions are made based on the approximative expression of input impedance. The validity of this logic has been demonstrated by the SPICE simulation of the synthesized circuit.

III. Implementation of the Design and Characterization Method

A design automation procedure has been developed to design and characterize LNA, the receiver first block, in CAIRO+ and using GiNaC for a chosen topology.

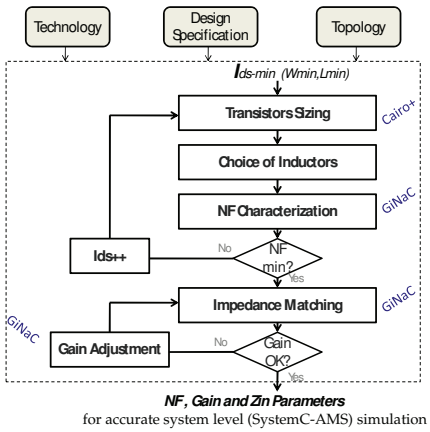


Fig. 5. Flow chart to implement the design and characterization method in a C++ environment

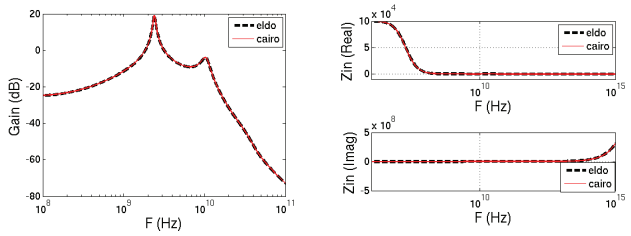
Using CAIRO+ and GiNaC, provides an automatic interaction between the system-level simulation and circuit-level design due to their unified environment. The same methodology can be applied to different topologies.

For a given topology, three symbolic admittance matrices are formed using the small signal equivalent circuit of transistors and on-chip inductors for NF, gain and input impedance. The synthesis flow is based on finding the current that gives the minimum noise figure of the transistors following by the choice of inductors to match the input impedance. However after impedance matching, the noise figure has been increased but we can guarantee that it would be the minimum possible noise figure for this topology. We design the load inductance to achieve the desired gain.

TABLE I

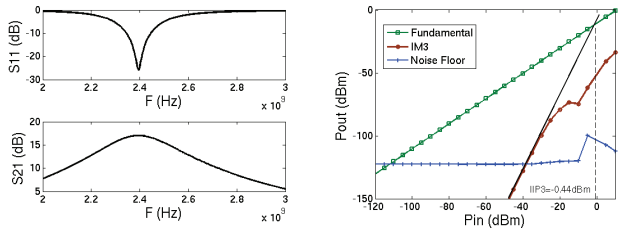
THE CIRCUIT PARAMETERS OF THE SYNTHESIZED 2.4GHZ AND 935MHZ LNAS WITH A COMPARISON BETWEEN THE AUTOMATICALLY CHARACTERIZED AND THE SIMULATED CIRCUIT PERFORMANCE.

Synthesized Circuit Parameters			Circuit Performance			
f_0 (Hz)	2.4 G	935 M	f_0 (Hz)		2.4 G	935 M
Wm1 (μm)	48.96	257.16	NF (dB)	CAIRO+	0.774	0.128
Wm2 (μm)	48.96	257.16		ELDO	0.727	0.279
Wm3 (μm)	5.08	25.89	Zin (Ω)	CAIRO+	50.00	50.00
R (Ω)	100K	100K		ELDO	49.57	47.23
R_{ref} (Ω)	1.811K	343.79	Gain (dB)	CAIRO+	19.14	18.65
L_{deg} (nH)	0.37	0.53		ELDO	19.04	18.49
L_g (nH)	48.65	67.37	S_{11} (dB)	ELDO	-24.24	-19.67
L_{out} (nH)	3	3	S_{21} (dB)	ELDO	17.028	17.126
I_{ds} (mA)	3.31	17.45	IIP3 (dBm)	ELDO	-0.44	-12.5



(a) (b)

Fig. 6. Perfect matching between simulation results and the automatically characterized SystemC AMS models of the synthesized 2.4GHz LNA (a) Gain (b) Input Impedance.



(a) (b)

Fig. 7. Simulation results of the synthesized 2.4GHz LNA: (a) S_{11}, S_{21} and (b) IIP3 at f_0= 2.4GHz.

The circuit-level design and characterization flow-chart is shown in Fig. 5. The design specifications consist of the central frequency, the desired gain and the source resistance. Avoiding the use of SPICE-like circuit-level simulators and implementing an automatic design, we have to characterize the circuit at the same time as we design it considering the contraints.

CAIRO+ provides a hierarchical sizing and biasing methodology for analog intellectual properties. It is used to size the transistors at a given DC operating point and also to compute the small signal parameters of transistors.

Characterizing a given circuit requires to solve the symbolic matrices, the size and complexity of which grow with the number of circuit nodes. Applying the symbolic computation by GiNaC would be helpful. Considering all the parasitic components, the results are as accurate as the SPICE simulation. The fact that admittance matrices are symbolic, makes it possible to take into account any parasitic components due to packaging or bonding wire.

Finishing the design procedure, we can return the characterized parameters to SystemC AMS for an accurate system-level simulation.

IV. DESIGN EXAMPLES

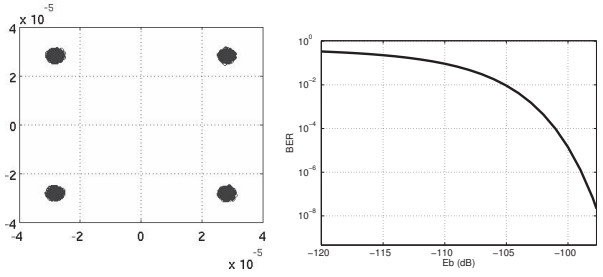
In this section, the results of two circuit design examples are represented with two different central frequencies of 2.4 GHz and 935 MHz using the 0.13μm CMOS technology with a power supply of 1.2 V.
Transistor lengths have been kept at minimum, the other synthesized circuit parameters and the performance of two

TABLE II

COMPARISON BETWEEN THE PERFORMANCE OF THE SYNTHESIZED 2.4GHZ LNA AND THE PERFORMANCE OF SEVERAL OTHER RECENT DESIGNS.

	Techno. (um)	NF (dB)	IIP3 (dBm)	Gain (dB)	S_{11} (dB)	S_{21} (dB)	P_{in} (mW)	V_{dd} (V)	I_{ds} (mA)	f_0 (Hz)	FoM
[9]	0.25	1.7	1.5	15	-	15	12	2.5	5	2G	205.92
[4]*	0.35	0.43	-2.87	19.8	-18	16	20	-	-	2.4G	212.42
[14]	0.18	0.77	-12.2	21.6	-17.7	-	11.2	1.8	-	2.4G	215.03
[15]	0.35	1.52	-4.3	20.2	-10.3	-	12.5	-	-	2.4G	210.51
[16]	0.25	2.5	0.5	14.7	-19.5	14.7	1.97	2	-	2.4G	213.09
[3]	0.13	0.76	-2.5	12	-6.5	12	4.2	1.2	3.5	2.14G	213.56
This work	0.13	0.72	-0.44	19.04	-24.24	17.02	3.8	1.2	3.16	2.4G	217.75

* Simulation results



(a) (b)

Fig. 8. Simulation results of automatically characterized SystemC AMS models showing the effect of the synthesized 2.4GHz LNA circuit noise on the performance of a complete QPSK RF receiver: (a) the constellation diagram for $P_{in} = -100dBm$ (b) The BER in function of the input power (P_{in}).

circuits for two frequencies are presented in Table I. The unconditional stability has been verified for two circuits.

Comparison with the other designs using the Figure of Merit (FoM) defined by (4) [17] is shown in Table II.

$$FoM = 10log(100(\frac{|S_{21}|_{(linear)} f_0^2}{(F-1)P_{dc(mW)}})) \quad (4)$$

In Fig. 6 the calculated and simulated gain are compared and the accuracy of the characterization of input impedance is shown. Fig. 7 represents simulated S-parameters and IIP3 respectively.

A QPSK-based RF transceiver is modeled and simulated using SystemC AMS at 2.4 GHz [6]. The automatically characterized models are used to obtain a high-level refined model taking into account circuit non-idealities [18]. The simulation results showing the constellation diagram and the Bit Error Rate (BER) in function of the input power of the receiver are shown in Fig. 8.

V. CONCLUSION

In this paper, an automatic design procedure for the synthesis of a cascode LNA with inductive source degeneration is presented. The design procedure is implemented in C++ using CAIRO+ for synthesis and GiNaC for characterization. Two LNA design examples operating at 2.4GHz and 935MHz were presented. LNA circuits generated using the proposed method have a Figure of Merit comparable to the state of the art. Perfect matching between simulation results and the automatically characterized models of the synthesized LNA was achieved to illustrate the proposed method. These models were then used in a high-level SystemC AMS simulation of a complete QPSK-based RF receiver to study the effect of the LNA noise figure on the Bit Error Rate of the receiver.

REFERENCES

[1] G. Tulunay and S. Balkir. "Synthesis of RF CMOS Low Noise Amplifiers". *International Symposium on Circuits and Systems, ISCAS*, pages 880–883, 2008.

[2] W. Cheng, A.J. Annema, and B. Nauta. "A multi-step P-cell for LNA design automation". *International Symposium on Circuits and Systems, ISCAS*, pages 2550–2553, 2008.

[3] D. Pienkowski. *"CMOS Low-Noise Amplifier Design for Reconfigurable Mobile Terminals"*. PhD thesis, Berlin University, 2004.

[4] A. Nieuwoudt, T. Ragheb, and Y. Massoud. "Narrow-band low-noise amplifier synthesis for high-performance system-on-chip design". *Microelectronics Journal*, pages 1123–1134, July 2007.

[5] A. Nieuwoudt, T. Ragheb, H. Nejati, and Y. Massoud. "Numerical Design Optimisation Methodoligy for Wideband and Multi-Band Inductively Degenerated Cascode CMOS Low Noise Amplifiers". *IEEE Transactions on circuit and systems*, vol. 56(No. 6):1088–1101, 2009.

[6] M. Vasilevski, F. Pecheux, N. Beilleau, H. Aboushady, and K. Einwich. "Modeling and Refining Heterogeneous System With SystemC-AMS: Application to WSN". *Design, Automation and Test in Europe, DATE*, pages 134–139, 2008.

[7] R. Iskander, M.M. Lourat, and A. Kaiser. "Automatic DC Operating Point Computation and Design Plan Generation for Analog IPs". *Analog Integrated Circuits and Signal Processing Journal*, vol. 56:93–105, 2008.

[8] *GiNaC is Not a CAS*. http://www.ginac.de/.

[9] D.M.W. Leenaerts, J. van der Tang, and C.S. Vaucher. *Circuit design for RF transceivers*. Kluwer academic publishers, 2001.

[10] D. Li and Y. Tsividis. "Active LC filters on silicon". *IEE Proceedings on Circuits, Devices and Systems*, vol. 147:49–56, 2000.

[11] B. Razavi. *RF Microelectronics*. Prentice Hall, 1997.

[12] Y.P.Tsividis. *Operation and modeling of the MOS transistor*. Mc Graw-Hill Book Company, 1987.

[13] J. Lucek and R. Damen. "Designing an LNA for a CDMA front end". *RF Design*, 1999.

[14] J.T. Yang, D.W. Shen, P.J. Tsai, and M.J. Wu. "A CMOS Radio Frequency Receiver for Bluetooth Applications". *1st Int'l Symposium on Quality Electronic Design-Asia*, pages 352–356, 2009.

[15] R. Ramzan, L. Zou, and J. Dabrowski. "LNA Design for on-Chip RF Test". *International Symposium on Circuits and Systems, ISCAS*, pages 4236–4239, 2006.

[16] I. Kwo and H. Shin. "Design of a New Low-Power 2.4 GHz CMOS LNA". *Journal of the Korean Physical Society*, vol. 40(No. 1):4–7, 2002.

[17] V. Chandrasekhar, C.M. Hung, Y.C. Ho, and K. Mayaram. "A Packaged 2.4GHz LNA in a 0.15mCMOS Process with 2kV HBM ESD Protection". *28th European Solid-State Circuits Conference, ESSCIRC*, pages 347–350, 2002.

[18] M. Vasilevski, H. Aboushady, and M.M. Louerat. "Automatic Model Refinement of GmC Integrators for High-Level Simulation of Continuous-Time Sigma-Delta Modulators". *IEEE International Symposium on Circuits and Systems, ISCAS*, 2009.