A 1.3V 26mW 3.2GS/s Undersampled LC Bandpass ΣΔ ADC for a SDR ISM-band Receiver in 130nm CMOS

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***Abstract*— This paper presents the implementation of an undersampled LC bandpass ΣΔ ADC with a raised-cosine feedback DAC. It directly converts after the LNA a signal centered in the ISM band at 2.442GHz with a sampling frequency of 3.256GHz. This circuit has been fabricated in a 130nm CMOS process, it occupies an area of 0.27mm^2 and is operating at a supply voltage of 1.3V. The Signal to Noise and Distortion Ratios measured are 34dB, 37dB and 42dB for respective bandwidths of 25MHz, 10MHz and 1MHz. The power consumption of the ΣΔ ADC is 26mW and its figure of merit is 2.3pJ/bit.**

I. Introduction

In the context of Software Defined Radio (SDR) receivers, an RF Nyquist Analog-to-Digital Converter (ADC) with a bandwidth of several GHz and high resolution is needed in order to be able to perform down-conversion and channel selection according to several standards in the easily programmable digital domain. RF receivers targeting multiple standards have so far used architectures based on RF sampling [1] in order to avoid using difficult and power hungry ADCs [2]. The conversion of only the band of interest of several MHz around the center frequency by using an LC bandpass ΣΔ modulator, as shown in Fig. 1, is a promising technique for realizing power efficient ADCs for SDR transceivers.

In order to simplify the digital down-conversion, the sampling frequency f_s of a bandpass ΣΔ modulator is usually chosen to be 4 times the center frequency, f_c [3]. Higher sampling frequencies have also been used to improve the maximum achievable Signal to Noise Ratio (SNR) [4]. Due to their high sampling frequencies, these ADCs have been implemented in SiGe BiCMOS technologies [3], [4]. In order to reduce the sampling frequency for a digital CMOS implementation, it has been proposed to apply the principle of undersampling bandpass signals to bandpass ΣΔ modulators [5]–[7]. In this case, the design of the modulator has to be done with extreme care to avoid deterioration due to aliasing.

In this paper, we report the first realization of an undersampled RF LC bandpass ΣΔ ADC in a standard low-cost CMOS technology, and moreover it is also the first implementation of a continuous-time ΣΔ with raised-cosine feedback DAC. The LC Bandpass ΣΔ ADC is centered in the ISM band at 2.442GHz with a sampling frequency reduced to 3.256GHz thanks to the undersampling technique.

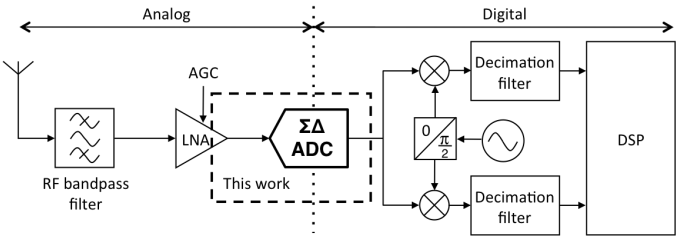

Fig. 1. RF receiver based on an LC bandpass ΣΔ ADC.

II. Undersampled Bandpass ΣΔ Modulators

Assuming that the sampling frequency of conventionnal bandpass ΣΔ modulators is usually $f_s = 4f_c$, the sampling frequency of undersampled bandpass ΣΔ modulators is defined as $f_{s_M} = \frac{4f_c}{M} = \frac{f_s}{M}$ with M the undersampling factor. The quantization noise is shaped around the frequencies $\frac{f_c}{M} + k\frac{f_{s_M}}{2}$, with k an integer, and since it is important that the ΣΔ modulator does not add noise in the vicinity of the input signal bandwidth centered around f_c, only odd values of the undersampling factor, M, can be used [7]. In our design we have an undersampling factor M= 3 which leads to a sampling frequency of $\frac{4f_c}{3} = 3.256$GHz.

As shown in Fig. 2, the ΣΔ output spectrum has a replica

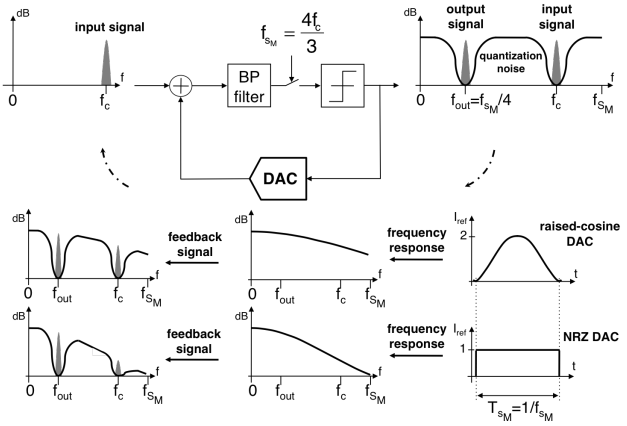

Fig. 2. Effect of the DAC transfer function on the feedback signal spectrum. Raised cosine DAC (top) and NRZ DAC (bottom).

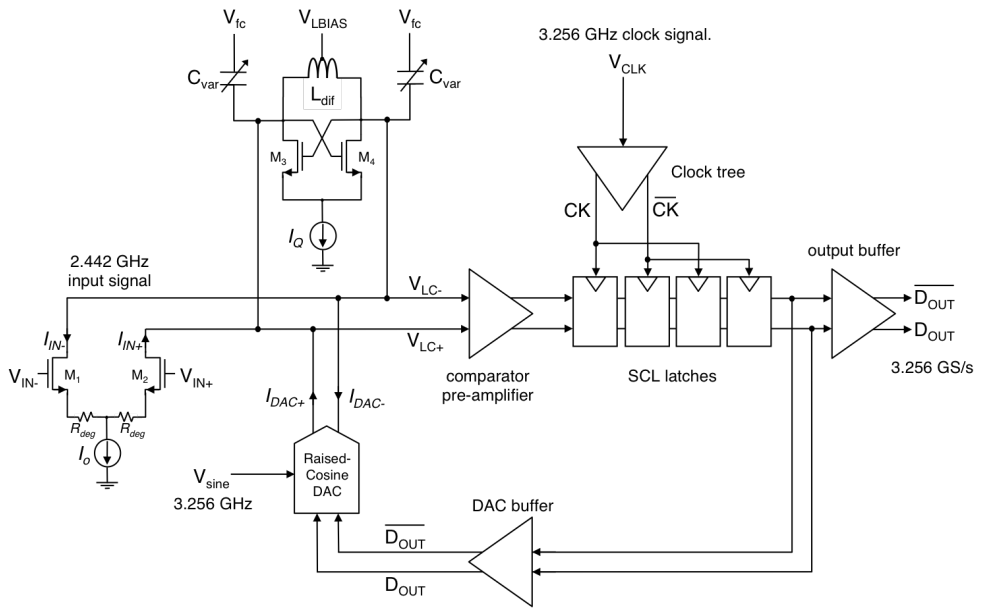

Fig. 3. Architecture of the second order undersampled LC bandpass $\Sigma\Delta$ ADC with raised-cosine feedback DAC.

of the input signal with the quantization noise shaped around $\frac{f_{s_M}}{4} = \frac{f_c}{3} = 814$MHz. This replica is considered as the output signal of interest since it can then be applied to the digital signal processing circuit for down-conversion and filtering. Nevertheless, for proper operation of the $\Sigma\Delta$ feedback loop, it is important to maintain the signal around the original center frequency, f_c, unaltered. As shown in Fig. 2, using an undersampled Non-Return-to-Zero (NRZ) DAC can significantly attenuate the signal components around f_c. The use of a raised-cosine DAC reduces this attenuation while avoiding the use of an up-conversion mixer in the feedback loop as proposed in [5], [6]. A raised-cosine DAC has also the important advantage of reducing SNR degradation due to clock jitter since its output signal slope is zero at the sampling instants, assuming that the raised-cosine signal and the comparator clock signal are locked together [8].

III. Circuit Design

Fig. 3 shows the architecture of the implemented second order single-bit undersampled LC bandpass $\Sigma\Delta$ ADC with raised-cosine feedback DAC. The input signal is applied to a transconductor composed of two transistors (M_1, M_2) and a current source, I_0, drawing 400μA. Two degeneration resistors, $R_{deg} = 435\Omega$ are used to improve the linearity of the input transconductor. For maximum SNR, the quality factor of the LC resonator centered at 2.442GHz is chosen to be equal to 80. The desired quality factor is higher than that usually used in similar LC based $\Sigma\Delta$ modulators, e.g. Q= 30 in [3] and Q= 11 in [4]. This is due to the fact that for a bandpass $\Sigma\Delta$ modulator, having an undersampling factor M, the effective quality factor of the $\Sigma\Delta$ loop filter, Q_{eff}, is M times lower than the quality factor of the loop filter without undersampling [7]. As shown in Fig. 3, the LC filter is composed of a differential inductor, $L_{dif} = 5.55$nH, having a quality factor of 14.48, and two varactors, $C_{var} = 1.2$pF. The quality factor enhancement is achieved using a negative resistance (M_3, M_4) externally tuned through its biasing current $I_Q = 400\mu$A. The resonance frequency is tuned using the biasing voltage V_{fc} of the varactors.

The comparator implementation is based on Source-Coupled-Logic (SCL) latches in order to cope with the sampling frequency of 3.256GHz. The latch clock signals are provided by a single-ended-to-differential circuit, which shapes an input sine wave V_{CLK} at 3.256GHz. The output buffer is an SCL inverter externally loaded with 150Ω resistors which are in parallel with the 50Ω impedance of the spectrum analyzer. An implementation of a differential raised-cosine current DAC is presented in Fig. 4. It is based on two sinusoidal current sources composed of transistors M_{P1} and M_{N1} driven by a 3.256GHz sinusoidal voltage source V_{sine}. For proper operation of the modulator and for minimum SNR

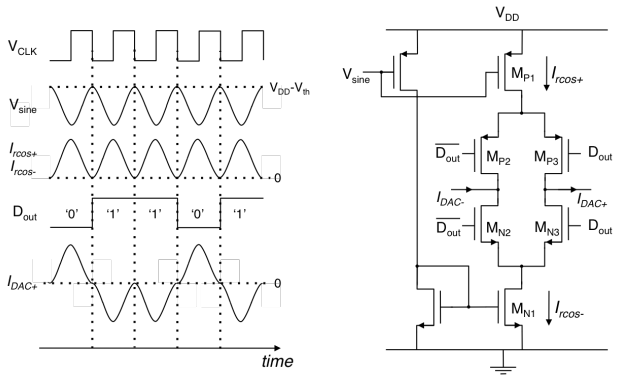

Fig. 4. Circuit and signals of the raised-cosine DAC.

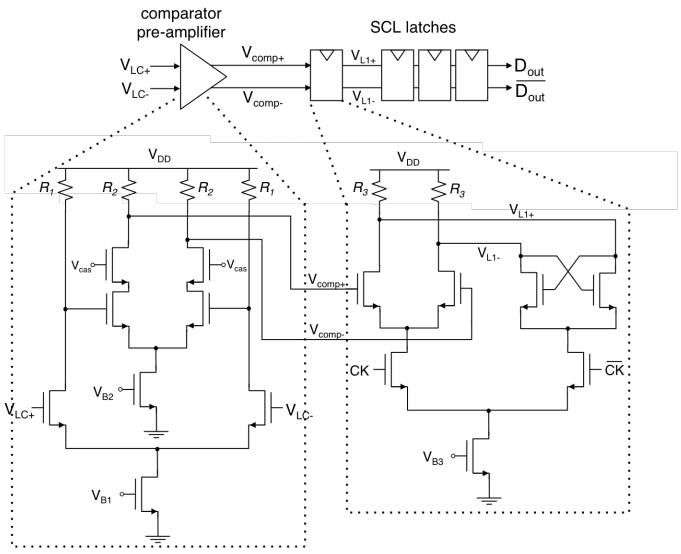

Fig. 5. Circuit of the comparator's pre-amplifier and the subsequent SCL latch.

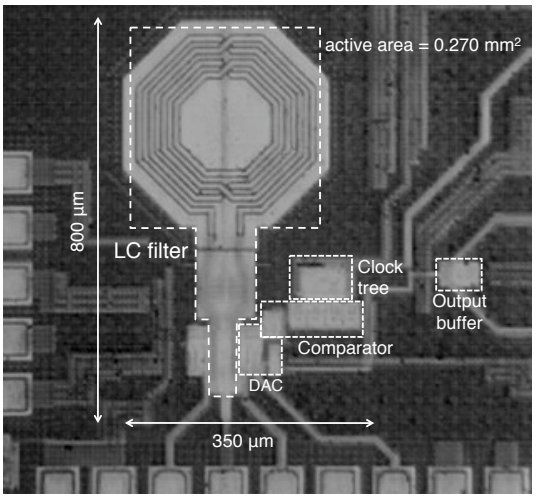

Fig. 6. Chip micrograph where the active area is 0.27mm^2.

degradation due to clock jitter, this sinusoidal voltage source is locked off-chip to the clock signal, V_{CLK}. As shown in Fig. 4, the sinusoidal currents I_{rcos+} and I_{rcos-} are diverted either to the +ve or the -ve output of the DAC through the NMOS ($\mathrm{M}_{N2}, \mathrm{M}_{N3}$) and the PMOS ($\mathrm{M}_{P2}, \mathrm{M}_{P3}$) switches. The raised-cosine DAC differential output signal $\mathrm{I_{DAC+}}$ and I_{DAC-} vary between $+80\mu$A and -80μA. The NMOS switches are directly driven by the SCL comparator output signal, which is between V_{DD} and $\frac{\mathrm{V}_{DD}}{2}$, whereas the PMOS switches are driven by the same signal shifted to $\frac{\mathrm{V}_{DD}}{2}$ and 0 using a level shifter.

Fig. 5 shows the circuit details of the comparator's pre-amplifier and the subsequent SCL latch. The preamplifier is composed of two stages of differential amplifiers with biasing currents of 1mA and 1.8mA. These amplifiers are loaded with resistors $\mathrm{R}_1 = 2.025\text{k}\Omega$ and $\mathrm{R}_2 = 600\Omega$. In the second stage, cascode transistors are used to reduce parasitic capacitances and kick-back noise. The pre-amplifier is followed by a cascade of four SCL latches. The last latches have higher biasing currents (1.8 mA) than the first ones (1.1 mA) in order to be able to drive the feedback DAC and the output buffers.

IV. Measurement Results

The chip micrograph is shown in Fig. 6. The prototype chip is fabricated in a 1P6M digital 130nm STMicroelectronics CMOS process. The active part of the chip is 0.27mm^2. A large area is occupied by the passive components. Fig. 7 shows the measured modulator output spectrum between 0 and $f_{s_M} = 3.256$GHz. An input signal has been applied at 2.45GHz and the replica due to the undersampling is at 806MHz. In this Figure, we can see that signals beyond $\frac{f_{s_M}}{2} = 1.628$GHz are attenuated. Fig. 8 is a zoom of the output spectrum in the band of interest, around $\frac{f_c}{3} = 814$MHz, it shows an image tone which could limit the maximum achievable SNDR if the modulator bandwidth is lower than 10MHz. For the targeted 25MHz band, this tone is below the noise floor. Fig. 8 also shows the measurement results of a 2-tone test used to indicate the intermodulation distortion. The plot in Fig. 9 shows the SNDR as a function of input signal power normalized to the highest power applied to the circuit. The measured SNDR values for bandwidths 25MHz, 10MHz and 1MHz were respectively 34dB, 37dB and 42dB. Operating with a 1.3V supply, the $\Sigma\Delta$ ADC consumes 26mW. The power efficiency Figure of Merit (FoM) is often calculated using the formula: $\text{FoM} = \frac{P}{2^{ENoB}\ 2BW}$, which is adapted to the lowpass converters since the power consumed P is only due to the bandwidth converted. In the case of the bandpass converters, we consider another FoM proposed in [9]:

$$\text{FoM}_{BP} = \frac{P}{2^{ENoB}\ 2BW(1+3\frac{f_c}{f_s/2})}$$

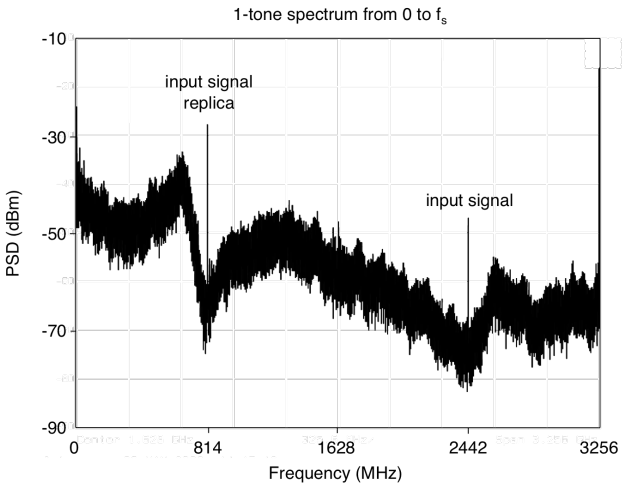

Fig. 7. Output signal spectrum from 0 to $f_{s_M} = 3.256$GHz.

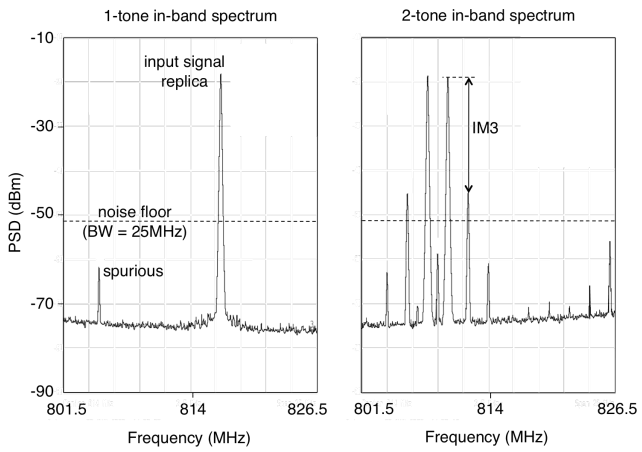

Fig. 8. 1-tone and 2-tone spectra of the $\Sigma\Delta$ output in the 25MHz band of interest around $\frac{f_c}{3} = 814$MHz.

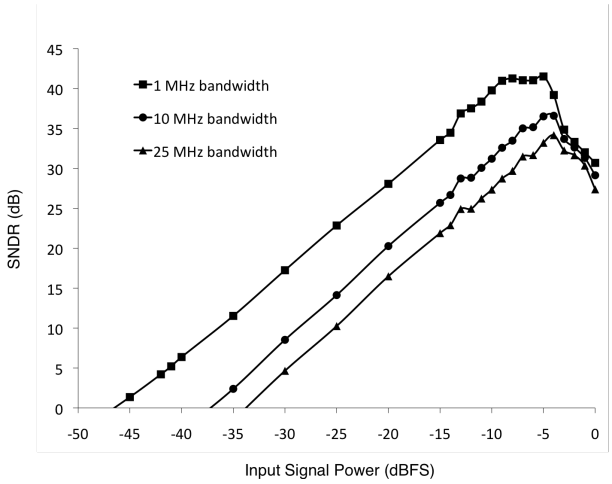

Fig. 9. SNDR versus input signal power for three bandwidths 1MHz, 10MHz and 25MHz.

TABLE I

CHIP PERFORMANCE SUMMARY.

Technology	130nm CMOS process
Active area (chip area)	0.35 x 0.8 mm^2 (1.32 x 1.26 mm^2)
Power supply	1.3 V
Center frequency	2.442 GHz
Clock rate	3.256 GHz
OSR (BW = 25 MHz)	65
SNDR / BW	34 dB / 25 MHz 37 dB / 10 MHz 42 dB / 1 MHz
SFDR (BW = 25 MHz)	32 dB
Total power consumption Filter and Input Gm DAC Comparator Clock Tree	26 mW 1.3 mW 1 mW 12.7 mW 11 mW

TABLE II

PERFORMANCE COMPARISON OF THE PROPOSED $\Sigma\Delta$ ADC WITH OTHER LC BP $\Sigma\Delta$ ADCS.

Reference	This work	[4]	[3]
order	2	4	4
SNDR (dB)	34	52	59
BW (MHz)	25	120	1
f_c (GHz)	2.442	2	0.950
f_s (GHz)	3.256	40	3.8
OSR	65	167	1900
Power (mW) @ V_{DD} (V)	26 @ 1.3	1500 @ 2.5	75 @ 2.5
Process	130nm CMOS	130nm SiGe BiCMOS	250nm SiGe BiCMOS
Area (mm^2)	0.27	2.4	1.08
FoM$_{BP}$ (pJ/bit)	2.3	15	20.7

The FoM$_{BP}$ of this chip for a bandwidth BW of 25MHz is 2.3pJ/bit. Table I summarizes the measured performance of the RF $\Sigma\Delta$ modulator and details the power consumed by each block. It can be seen that 42% of the power is dissipated in the clock tree used to sharpen the clock edges.

As depicted in table II, in comparison with other recently reported implementations, this RF bandpass $\Sigma\Delta$ ADC is at least 84% more power efficient, it converts a signal centered at a frequency at least 20% higher and it occupies an area at least 70% smaller.

V. CONCLUSIONS

In this paper, we report the first implementation of an undersampled RF LC bandpass $\Sigma\Delta$ modulator with raised-cosine feedback DAC, paving the way to quasi-fully digital SDR receivers. The circuit is realized in a standard low-cost 130nm CMOS process operating at 1.3V supply. Compared to recently published implementations, this circuit has the lowest figure of merit.

REFERENCES

[1] F. Montaudon et al. "A Scalable 2.4-to-2.7GHz Wi-Fi/WiMAX Discrete-Time Receiver in 65nm CMOS". In *IEEE ISSCC*, February 2008.

[2] M. Choi, J. Lee, J. Lee, and H. Son. "A 6-bit 5-GSample/s Nyquist A/D Converter in 65nm CMOS". In *IEEE Symposium on VLSI Circuits*, June 2008.

[3] B.K. Thandri and J. Silva-Martinez. "A 63 dB SNR, 75-mW Bandpass RF $\Sigma\Delta$ ADC at 950 MHz Using 3.8-GHz Clock in 0.25-m SiGe BiCMOS Technology". *IEEE Journal of Solid-State Circuits*, 42, February 2007.

[4] T. Chalvatzis, E. Gagnon, M. Repeta, and S.P. Voinigescu. "A Low-Noise 40-GS/s Continuous-Time Bandpass ADC Centered at 2 GHz for Direct Sampling Receivers". *IEEE Journal of Solid-State Circuits*, 42, May 2007.

[5] F. Gourgue, M. Bellanger, S. Azrouf, and V. Bruneau. "A bandpass subsampled delta-sigma modulator for narrowband cellular mobile communications". In *IEEE ISCAS*, May 1994.

[6] A.I. Hussein and W.B. Kuhn. "Bandpass $\Sigma\Delta$ Modulator Employing Undersampling of RF Signals for Wireless Communication". *IEEE Transactions on Circuits and Systems II*, 47, July 2000.

[7] A. Kammoun, N. Beilleau, and H. Aboushady. "Undersampled LC Bandpass $\Sigma\Delta$ Modulators with Feedback FIRDACs". In *IEEE ISCAS*, May 2006.

[8] S. Luschas, R. Schreier, and H. Lee. "Radio Frequency Digital-to-Analog Converter". *IEEE Journal of Solid-State Circuits*, 39, September 2004.

[9] I. Galdi, E. Bonizzoni, P. Malcovati, G. Manganaro, and F. Maloberti. "40 MHz IF 1 MHz Bandwidth Two-Path Bandpass $\Sigma\Delta$ Modulator With 72 dB DR Consuming 16 mW". *IEEE Journal of Solid-State Circuits*, 43, July 2008.