

Wide-Band Continuous-Time $\Sigma\Delta$ Modulator With VCO Quantizer

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Abstract—A methodology for the design of Continuous-Time (CT) Sigma-Delta ($\Sigma\Delta$) modulators with VCO-based quantizer is proposed. The coefficients of the CT $\Sigma\Delta$ modulator are accurately calculated such that the noise transfer function of the modulator is exactly the same as a Discrete-Time (DT) $\Sigma\Delta$ modulator of the same order. Several design examples for different modulator orders and feedback DAC signal shapes are given to validate the proposed methodology.

I. INTRODUCTION

Modern wireless communication systems require high performance A/D converters with increasing bandwidth and resolution. Sigma-Delta modulators are usually used for high resolution while the use of multi-bit quantizers is necessary to maintain the high-resolution at wide-band operation.

A Continuous-Time (CT) Sigma-Delta ($\Sigma\Delta$) modulator with a VCO-based quantizer is shown in Fig. 1. Time domain quantizers, such as VCO-based [1] are potential candidates for modern CMOS technology due to the fact that they are less sensitive to supply voltage reduction compared to conventional voltage quantizers.

In this work, a systematic method is proposed to calculate the coefficients of a CT $\Sigma\Delta$ modulator with VCO-based quantizer considering loop delay compensation [2]. This technique is based on the discrete-time to continuous-time (DT-CT) equivalence [3].

In section II, the VCO-based quantizer model is described. Section III presents the proposed design methodology. In section IV design examples and simulation results are presented for several modulator orders and feedback DAC waveform shapes. The conclusion is presented in section V.

II. VCO-QUANTIZER MODEL

The VCO-based quantizer architecture used is shown in Fig.2. The main idea is to count the number of inverters switching state within the clock period by comparing samples of their current and previous states. The inverters delay is set by the input tuning voltage. Each clock cycle, the number of inverters switching state will represent the input tuning voltage while the total number of inverters (N) defines the quantizer resolution.

Fig. 3 represents the linear model describing the architecture.

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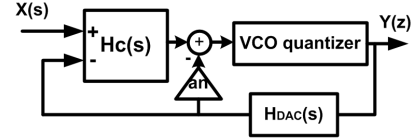


Fig. 1. Continuous-Time $\Sigma\Delta$ modulator with VCO-based quantizer.

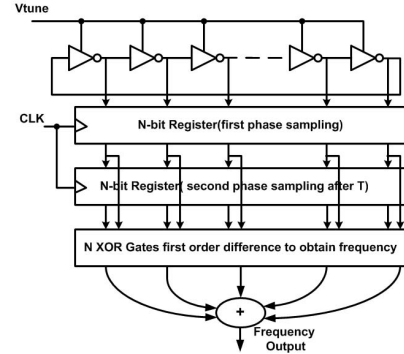


Fig. 2. VCO-based quantizer architecture.

III. DESIGN METHODOLOGY OF CT $\Sigma\Delta$ WITH VCO-BASED QUANTIZER

The discrete-time to continuous-time transformation [3] determines the coefficients of an N^{th} order CT $\Sigma\Delta$ modulator with the same Noise-Transfer-Function (NTF) of a DT $\Sigma\Delta$ modulator of the same order. This is done by comparing their respective noise transfer functions $NTF_c(z)$ and $NTF_d(z)$.

$$NTF_d(z) = \frac{1}{1 - G_d(z)} \quad (1)$$

$$NTF_c(z) = \frac{Y(z)}{E_v(z)} = \frac{(1 - z^{-1})}{1 - G_c(z)} \quad (2)$$

where $G_d(z)$ and $G_c(z)$ are the corresponding loop gains for the DT and the CT modulators respectively.

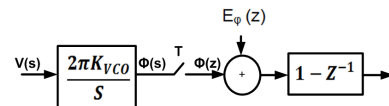


Fig. 3. Linear model of a VCO-based quantizer

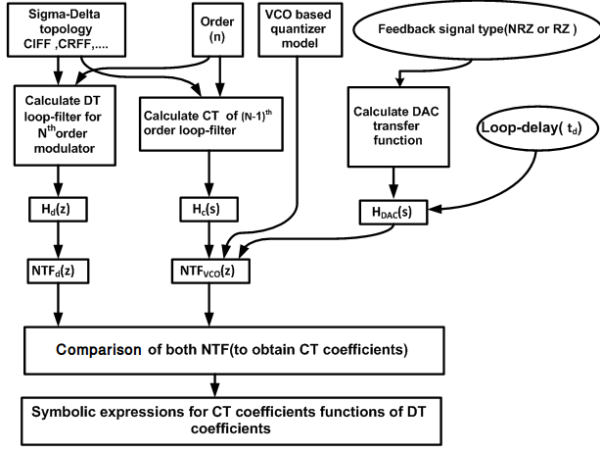


Fig. 4. The flowchart of the proposed systematic design methodology.

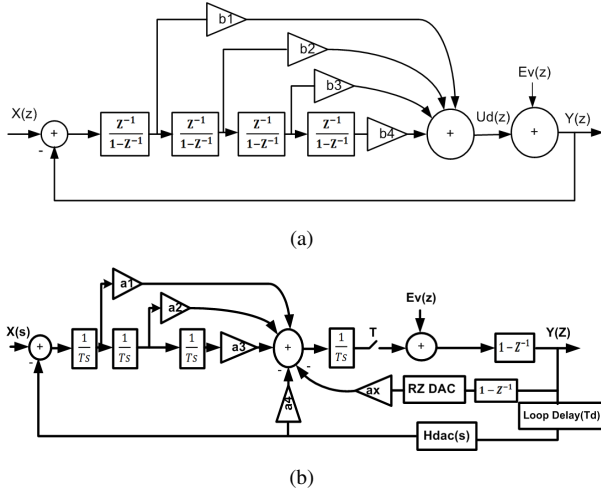


Fig. 5. 4^{th} order $\Sigma\Delta$ modulator CIFF (a) DT (b) CT

Through symbolic equivalence between $NTF_c(z)$ of (2) and $NTF_d(z)$ of (1), the coefficients of similar z orders are equated. Hence the CT $\Sigma\Delta$ modulator coefficients are determined.

IV. SYSTEM LEVEL SIMULATION RESULTS

A. Design Example With Ideal VCO model

In order to verify the proposed design methodology, a 4^{th} order DT $\Sigma\Delta$ modulator with 4-bit quantizer is designed using Schreier Delta-Sigma toolbox for the following wide-band specifications: $OSR=16$, $bandwidth=20$ MHz and $f_s=640$ MHz. Fig. 5(a) shows the 4th order DT $\Sigma\Delta$ modulator linear model using a Cascade of Integrators in Feedforward (CIFF) architecture while the CT $\Sigma\Delta$ modulator equivalent model with VCO-based quantizer and loop delay compensation is shown in Fig. 5(b).

The SNR plot versus the input amplitude in dB for both modulators is shown in Fig. 6. In order to verify the generality, SNR curves are traced as shown in Fig. 6 for other design examples. The curves traced from system level simulations

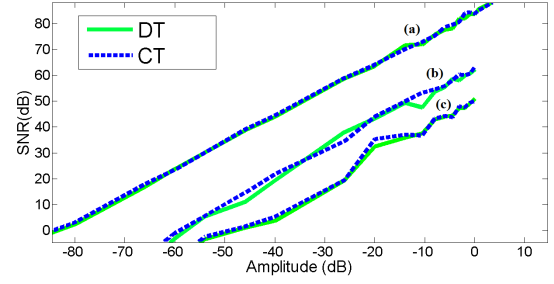


Fig. 6. SNR plot with input amplitude in dB for DT $\Sigma\Delta$ modulator and CT $\Sigma\Delta$ modulator with VCO quantizer (a) 4^{th} order with loop and NRZ DAC (b) 3^{rd} order with resonator and NRZ DAC (c) 2^{nd} order with RZ DAC

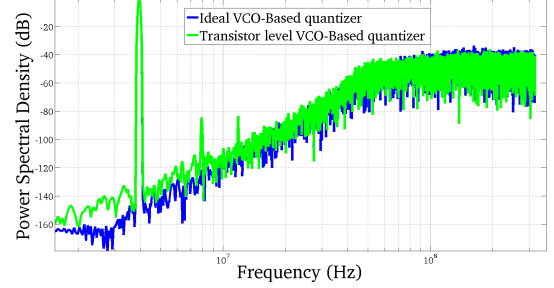


Fig. 7. Output power spectral density of a transistor level 4^{th} order CT $\Sigma\Delta$ modulator with VCO-quantizer with NRZ DAC.

verify the equivalence of DT and CT models designed with the proposed methodology.

B. Transistor Level Simulation and VCO Non-linearity

The VCO-based quantizer is described in transistor level using $0.13 \mu\text{m}$ CMOS technology. Active RC integrators are used while DACs are ideally modeled. The output power spectral density from simulation of the CT $\Sigma\Delta$ modulator with VCO-based quantizer is shown in Fig. 7. The VCO non-linearity appears as a harmonic distortion in the output spectrum. The total Signal-to-Noise-and-Distortion-Ratio (SNDR) for this simulation is 65 dB.

V. CONCLUSION

In this paper, we presented a generalized method for the determination of the coefficients of CT $\Sigma\Delta$ modulator with VCO-based quantizer. A design example is presented for a 4^{th} order modulator with 4-bit quantizer in $0.13 \mu\text{m}$ CMOS technology. VCO non-linearity is the limiting factor for the maximum SNDR achieved.

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