

Design and Modeling of 8-Bit Successive Approximation Analog to Digital Converter

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Abstract—This paper presents a functional design and modeling of a successive approximation analog to digital converter(SAR ADC). The SAR ADC is described in VHDL-AMS behavior models and transistor level circuit netlists using the $0.13\mu m$ technology and supply voltage equals to 1.2V. The system was simulated using a signal commercial simulator.

I. INTRODUCTION

The trends in many energy-limited applications such as MEMS sensors ,micro-robotics and wireless sensor network add more challenges to reduce the power consumption. Power saving can be achieved in ADC by choosing the best architecture level among different ones presented. One of the most known ADC architecture for low power application is the Successive Approximation ADC. In this paper, we have a mixed simulation that contains behavior models simulation like the control unit and real circuits simulation like the comparator and the Digital to Analog Converter (DAC). In section II, We will see the architecture of the system and how it works. In section III, the model simulation results will be shown.

II. SAR ADC ARCHITECTURE

In Fig. 1, we can see how the different parts of the SAR ADC are connected. In our topology, the signal is sampled in the *first clock cycle* and is converted in the *next N clock cycle*, where N is the *number of bits*. We use the DAC in the first clock cycle for Sampling the signal so that we decrease the active blocks in our architecture to reduce the power consumed. Our DAC contains two chains of binary weighted capacitors so that we sample the signal in a differential way . The differential outputs of the DAC are connected to the comparator input terminals as in Fig. 2 and the comparator output is connected to the control unit that controls the switches in the DAC that connect the capacitors terminals to the three references ; the supply voltage V_{dd} , the common mode voltage $V_{cm} = V_{dd}/2$ and the ground. This architecture was described in [1] and [2].

A. SAR ADC Modes

In the first half cycle of the first clock cycle, The DAC capacitors bottom plates in the 2 chains are connected to the input signal while the top plates are connected to $V_{dd}/2$, *this is the sampling mode* as in Fig. 2. In the second half all bottom plates are connected to $V_{dd}/2$, *this is the inversion mode*. After the first cycle, the control unit sees if the output

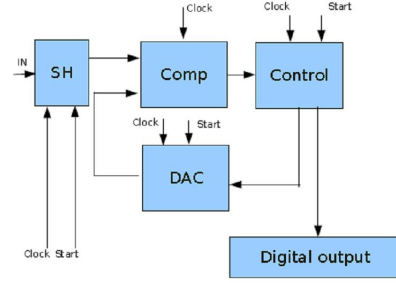


Fig. 1. SAR ADC architecture

of the comparator (comp_out) is high, it connects the biggest capacitor bottom plate to V_{dd} in the bottom chain and the biggest capacitor bottom plate to gnd in the upper chain, if comp_out is low, the control unit makes the opposite, this mode is called *charge redistribution mode* that happens in N clock cycle with each capacitor in both chains. Finally the digital output is corresponding to the output of the comparator in each clock cycle in the charge redistribution mode.

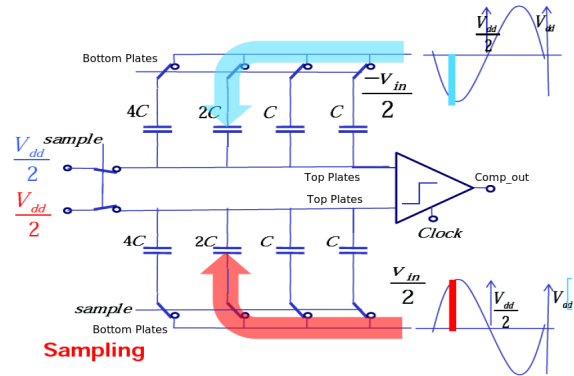


Fig. 2. Sampling Mode in SAR ADC with 4 bits

B. Comparator Circuit

The comparator in Fig. 3 is described by a spice netlist. It is synchronous with the clock Clk , it compares the 2 terminals of the DAC; $V_{DACBottom}$ that is connected to the negative terminal and V_{DACTop} that is connected to the positive terminal. The widths of the transistors are calculated

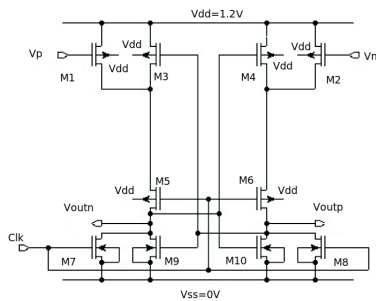


Fig. 3. Comparator Circuit

using a tool called CHAMS [3]. With this tool, we can precise the technology, the current, the nodes voltages and the length of each transistor thus we can design the transistors M1 and M2 to amplify the input signal and the transistors M3, M4, M9 and M10 to be back to back inverters that work depending on the differential input signal as in Fig 4, so we can control the power consumption and the transconductance needed. Both comparator outputs are connected to a latch to keep the comparator output constant every clock cycle.

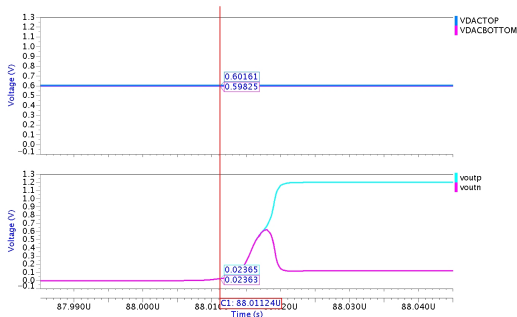


Fig. 4. Comparator Output Before The Latch

C. Control Unit VHDL-AMS Behavior Model

The control unit takes the output of the comparator to send control signals to the switches in the DAC. At sampling mode, it send signals so that the upper plates of both chain are connected to $V_{dd}/2$ and the bottom plates are to V_{in} then at inversion mode it send signals so that the bottom plates are connected to $V_{dd}/2$. In each clock cycle of the charge redistribution mode, depending on comparator output, The control unit decides either to connect the corresponding weighted capacitor bottom plate in the bottom chain to V_{dd} and the corresponding weighted capacitor bottom plate in the top chain to gnd or the opposite, So we increase or decrease the voltages on the top plates of both chains by binary weighed level voltage ($V_{dd}/4, V_{dd}/8, \dots, V_{dd}/256$). This block was described in VHDL-AMS.

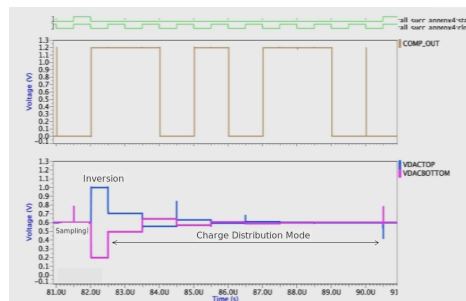


Fig. 6. Simulation Results

D. Digital to Analog Converter Circuit

The model of the DAC is a spice netlist that contains 8 binary weighted capacitors in each chain, the top plates are

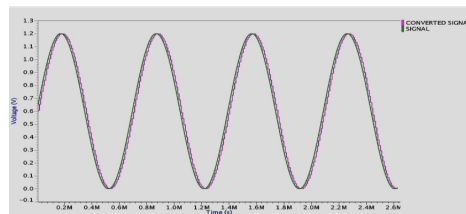


Fig. 7. The Input Signal and The Output Converted Signal

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