

SYSTEMATIC DESIGN OF A SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERTER

By
Eng. Mootaz Bellah Mohamed Mahmoud Allam
B.Sc. in Electronics and Communications Engineering – Ain Shams University

A Thesis Submitted to the
Faculty of Engineering at Cairo University
in Partial Fulfillment of the Requirements for the Degree of

MASTER OF SCIENCE

in
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2008

Dedication

To My parents who dedicated all their lives, love and care for me and my brother.

Acknowledgements

First of all, thanks GOD for your help throughout my whole life. For so many times, I felt helpless but You always guided me through all difficulties.

I would like to thank my supervisors in Egypt Prof. Amr Badawi from Cairo University and Dr. Mohamed Dessouky from Ain Shams University, for their patience, support and useful comments.

Very special thanks to my supervisor in France, Dr. Hassan Aboushady from University Paris 6, for hosting me for 5 months in LIP6 and for his continuous support, advices and long conference calls in very critical moments.

Words are not enough to thank my mother, father and brother for their care, love and sacrifices. They are always there when I need them and without their advices and love i wouldn't have gone any far.

I would like also to thank Prof. Hani Ragai from Ain Shams University whom I owe all my technical knowledge in the field of integrated circuits, as well as the teaching and life knowledge which I acquired while tutoring for his classes during 3 years in the French university.

Many thanks to Prof. Yehya Bahnas from Cairo University who kindly helped me get through all the administrative procedures during the thesis.

I am very grateful to Prof. Taha Abdallah, the Dean of the faculty of engineering of the French University for his flexibility and encouragement and Dr. Fabien Flori, the faculty international coordinator, for his confidence and efforts for my Ph.D arrangements.

Special gratitude and many thanks to Mme. Marie-Minerve Louerat and Mr. Jacky Porte from LIP6 laboratory of University Paris 6, for their valuable notes and comments.

I would like to thank my best friend Mohamed Wisam Farouk for his serious efforts in the manuscript revision and my defense preparation.

I would like equally to thank Rami Iskander, Nicolas Beilleau and Diomadson Belfort from the analog integrated circuits team of LIP6 for the support with the laboratory tools during my stay in Paris. Deep Thanks to Amr Misbah from Ain Shams University for support with models, technology and tools.

Finally, I am very thankful to my best friends and coworkers for understanding and rich conversations: Ahmed Shakib, Mohamed Said, Ahmed Aly, Rania elanwar, Mohamed Sabet, Abdallah Omar, Georges Ishac and Amr elshazly.

Abstract

New emerging communication systems and applications place very stringent requirements on energy consumption. Such requirements led to exploiting a portion of the analog-to-digital converter design space that has received little attention in the past decade, namely moderate resolution and speed, yet very low power ADCs. Those ADCs are critical components in large-scale wireless sensor networks used in a large set of applications ranging from tracking wildlife populations to measuring and predicting weather patterns. The successive approximation analog-to-digital converter with its minimal analog circuitry, emerges as a potential candidate to satisfy their low power specifications.

In this thesis, a systematic design methodology for a successive approximation analog-to-digital converter is presented with emphasis on the analog design reuse techniques. A general multiple abstraction simulation environment is developed in VHDL-AMS to describe and simulate the whole mixed ADC blocks. The analog circuit synthesis tool COMDIAC ¹ and the analog layout generation language CAIRO ² developed in LIP6 ³ are used in the design cycle. A case study of a low-power 8-bit SA-ADC in ST 0.13 μm technology with MIM capacitors is realized from system to layout with special attention to component matching. The analog part of the converter consumes 0.72 μW for 7.6 bit ENOB on 0.122mm² active area. The FOM is 33fJ per conversion-step.

Keywords: Data Converters, Successive Approximation, Common Centroid, Wireless Sensor Networks, Analog Design Automation.

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Introduction

1.1 New Challenges in ADC Design

Trends in many energy-limited applications and communication systems, such as wireless sensor networks, micro-robotics and software defined radios, add more design challenges to improve flexibility, system integration and bandwidth efficiency, yet with lower power consumption and smaller area to meet cost target [1]-[2]-[3]-[4]-[5]-[6]. Typical requirements of these systems architectures are met with a medium-resolution, low power consumption analog-to-digital converter (ADC) to extend the duration of the system battery power operation. Extending the ADC bandwidth to handle wide band RF signals under these constraints represents a major challenge.

Power saving can be achieved at both system architecture and circuit level design. At the architecture level, different ADC topologies consume different power for the same specifications. The successive approximation ADC exhibits the lowest power consumption reported in literature due to its minimal active analog circuit requirement [7]-[8]-[9]. At the circuit level, decreasing the supply voltage is an effective way to realize a low power design. The power of digital circuits directly benefits from supply voltage reduction. However, the low supply voltage makes the analog circuit design more difficult. For instance, when the sum of the absolute value of the NMOS threshold voltage and that of the PMOS is larger than the supply voltage, conventional analog switches made of transmission gates may not be fully turned on as in the case of higher supply voltages. This state of sub-threshold conduction implies poor conductivity thus limiting the circuit bandwidth. In addition, some useful design techniques such as cascoding and gain boosting may not be applicable because of the limited signal swing. Additional circuitry and techniques should be used, thus complicating the analog circuit design at reduced supply voltages.

1.2 Design Automation and Analog Design Reuse

The current complexity of integrated electronic circuits makes it important for a designer to reuse his designs in many technologies with no need to repeat the process of design each time. This technology portability feature has been successful on the digital side of mixed signal systems but is still extremely difficult to achieve in the

analog counterpart of these systems because of the multi-dimensional analog design space. Accordingly, embedding pre-characterized and pre-verified, reusable analog cores in SoC is becoming more appealing in order to reduce SoC time-to-market.

1.3 Objectives

This work explores architectural strategies and circuit techniques, focusing on identifying the main difficulties and the complete design parameters. This is required to offer a systematic design approach for a successive approximation SA-ADC from the system level to the layout level with emphasis on analog design automation techniques. The major axis of this thesis can be summarized in the following points:

- Studying SA-ADC architectures and key design parameters ending up with the proposed systematic design approach.
- Establishing a general simulation platform for the full ADC mixed blocks with multiple levels of abstraction, allowing to characterize each block with all possible descriptions from ideal to technology models.
- Exploiting design automation techniques to automate the majority of the ADC design flow at the circuit and layout level
- Applying the design methodology to a case study with specifications suitable for wireless sensor nodes

1.4 Outline

This section gives a brief overview of the contents of the following chapters: After a brief introduction in Chapter 1 and statement of the main objectives and thesis organization, Chapter 2 presents a background on the modern analog-to-digital converters in terms of specifications and performance evaluation, a brief comparison of the state-of-the-art Nyquist converters and the motivation for reviving successive approximation ADC.

In Chapter 3, the system block diagram and the functionality are shown, the architecture and algorithm are presented then the detailed operation of an SA-ADC is illustrated for both single ended and differential implementations. Finally, system level simulation results are presented with VHDL-AMS ideal descriptions for different resolutions with the corresponding control flowcharts.

Chapter 4 discusses the circuit level design with thorough analysis for the different blocks architectures of the ADC at the transistor level. The non-idealities, the circuit design trade offs and the factors limiting accuracy and speed are presented.

Based on the discussions of Chapter 4, Chapter 5 presents the proposed systematic design methodology for the SAR-ADC then introduces analog circuit automated design tool COMDIAC [10] and analog layout generation tool CAIRO [11] with examples. A common centroid automatic placement algorithm [12] is used for maximum capacitor matching.

To verify the former systematic design methodology, Chapter 6 presents a case study: A low-power successive approximation ADC is designed from system specifications to layout generation with specifications for wireless sensor nodes applications. A general multiple abstraction simulation environment developed in VHDL-AMS and matlab is used to launch sets of automated ADC performance analysis. Special component matching techniques are used in Layout. Finally, a comparison with the state-of-the-art realizations is held with a discussion of layout generation results.

Finally Chapter 7 summarizes the objectives achieved and concludes the thesis with possible directions for future work.

General ADCs Specifications

2.1 Introduction

In this chapter, a background on the main operations of the analog to digital converters is presented in section 2.2 . The converters specifications and the performance parameters are stated in section 2.3. The power efficiency of different Nyquist ADCs is discussed in section 2.4. Finally, the state-of-the-art Nyquist converters are presented in section 2.5.

2.2 ADCs Main Operations

The basic operation of an analog-to-digital converter (ADC) is divided into four elementary steps. As shown in Fig. 2.1, those main functions are: continuous-time anti-aliasing filtering, sampling, quantizing and data coding. This section will illustrate those functions and their effect on signals.

2.2.1 Sampling

Fig. 2.2 shows the operation of an ideal sampler, yielding a sequence of delta functions whose amplitude equals the signal at the sampling times. For uniform sampling with period T , the sampler output is given by:

$$x^*(t) = x^*(nT) = \sum x(t)\delta(t - nT) \quad (2.1)$$

Eq. 2.1 outlines the inherent non-linearity of the sampling process (multiplication is a non-linear operation). So the sampled data version, as stated by Eq. 2.1 is made by the superposition of weighted deltas. However a practical circuit does not

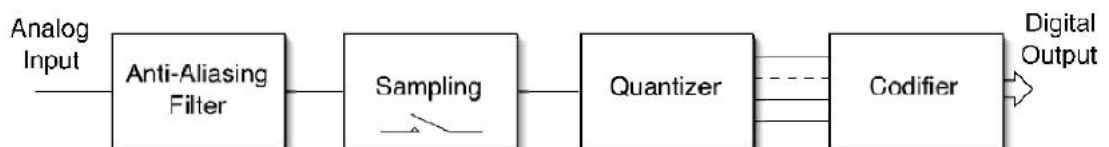


Figure 2.1: Elementary blocks of an ADC

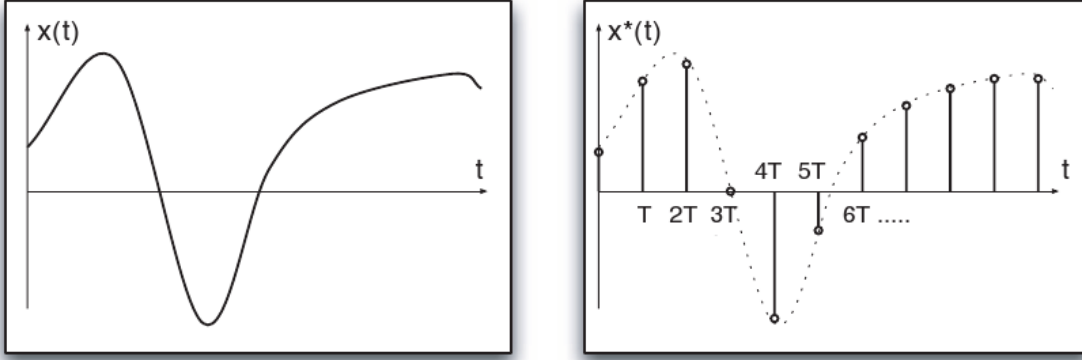


Figure 2.2: Ideal sampling: continuous time to discrete time

generate deltas but pulses with finite duration and amplitudes equal to the input at the sampling instances. Regardless of the pulse shape and duration, the pulses are intended to represent the input only at the exact sampling instances nT . Then the Laplace transformation of the sampled signal is

$$L|x^*(nT)| = \sum_{-\infty}^{\infty} (X(s - jnw_s)) \quad (2.2)$$

Eq. 2.2 shows that the spectrum of $x^*(nT)$ is the superposition of infinite replicas of the input spectrum, centered at multiples of the sampling frequency and being shifted along the f axis by $nf_s (= n/T)$ where $n = 0, \pm 1, \pm 2, \dots$. As a result the spectrum is periodic with period f_s . That transformation of the input spectrum from band-limited into an infinite replica reveals once more the non-linear nature of sampling.

Assuming that the bilateral spectrum of the input signal is the one in Fig. 2.3 (a) with two peaks at f_1 and f_2 and vanishing at frequencies higher than f_B . In Fig. 2.3 (b), the sampling frequency is higher than two times f_B (oversampling), there's no interference of the replicas and the restoration of the signal is possible through filtering. But in the case of Fig 2.3 (c) where $f_s < 2f_B$, the replicas partially overlap and the spectrum alteration makes it impossible to preserve the continuous-time features. The role of the continuous-time anti-aliasing filter placed before the sampler is thus to prevent unwanted noise and interferences laying outside the signal bandwidth which could add up in the signal bandwidth through the sampling operation.

According to the previous discussion, the condition to restore the sampled signal is that the signal largest frequency component $f_B < f_s/2$ which is defined as the Nyquist frequency. The restored signal in terms of the sampled is

$$x(t) = \sum_{-\infty}^{\infty} x(nT) \frac{\sin(w_s(t - nT)/2)}{w_s(t - nT)/2} \quad (2.3)$$

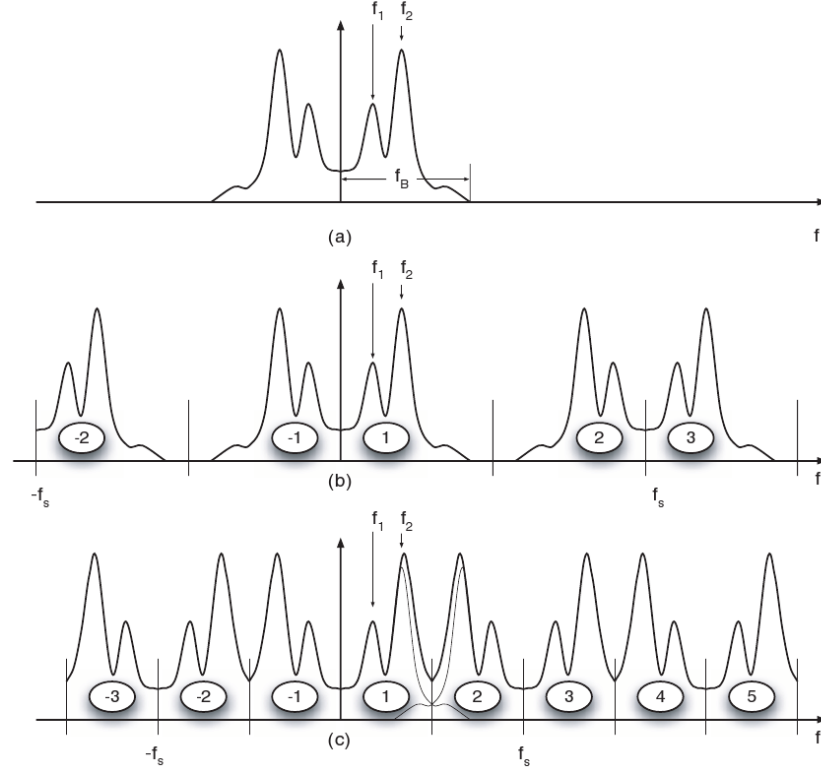


Figure 2.3: Signal Spectrum (a) Continuous time (b) Oversampled (c) Undersampled

Data converters using $f_s \gg 2f_B$ are called "Oversampled converters" and the most important of those converters is the $\Delta\Sigma$ -ADC. But the ADCs using $f_s = 2f_B$ are called "Nyquist rate converters" like the pipeline, flash and the successive approximation.

2.2.2 Quantization Noise

Amplitude quantization is the change of a sampled data signal from continuous level to discrete level. The dynamic range of the ideal quantizer is divided into a number of equal quantization intervals, each of which is represented by a given analog amplitude. An input amplitude that resides within a certain quantization interval is converted to the analog amplitude representing this interval. Often the value representing a quantization interval is the mid-point of the interval. In some cases, either the upper or the lower bound represent the interval.

Assuming that $X_{FS} = X_{max} - X_{min}$ is the full scale range of the quantizer and M is the number of quantization intervals; the amplitude of each quantization step (interval), Δ , is

$$\Delta = \frac{X_{FS}}{M} \quad (2.4)$$

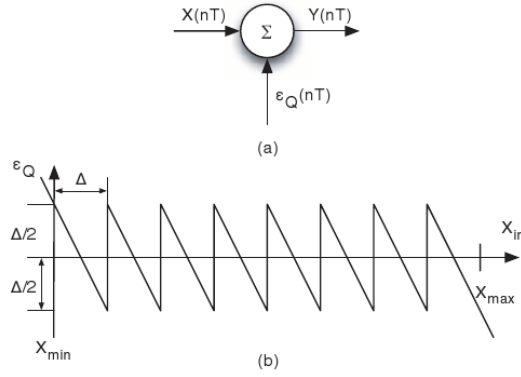


Figure 2.4: Quantization error

Since the mid point of the n -th interval $X_{m,n} = (n + 1/2)\Delta$ represents all the interval amplitudes, quantizing an input level other than $X_{m,n}$ leads to a quantization error, ϵ_Q . This unavoidable error becomes zero only when the number of bits tend to infinity which is practically unfeasible. The output Y of a quantizer with input X_{in} is

$$Y = X_{in} + \epsilon_Q = (n + 1/2)\Delta; \quad n\Delta < X_{in} < (n + 1)\Delta \quad (2.5)$$

Fig. 2.4 (a) illustrates the quantization process. The quantization error ϵ_Q is added to the input to obtain the quantized output. The addition is a linear operation but the added term is a non-linear function of the input. Fig. 2.4 (b) shows that the quantization error ϵ_Q ranges from $-\Delta/2$ to $\Delta/2$ for the case where each interval is represented by its mid point. Outside the dynamic range $X_{min} \dots X_{max}$ the output of the quantizer saturates to the two bounds and the quantization error continues to increase linearly in the positive and negative directions. A binary code is the most likely used to represent an ADC quantization interval.

It is needed to study the ADC capability of preserving the signal features after quantization. This implies finding a way to model this quantization effect. As is known, the effect of the noise is quantified by the signal-to-noise ratio (SNR) defined by

$$SNR|_{dB} = 10 \cdot \log \left[\frac{P_{sig}}{P_{noise}} \right] \quad (2.6)$$

Where P_{sig} and P_{noise} are the power of the signal and the power of the noise in the band of interest. When studying the effect of quantization it can be convenient using the SNR concept and considering the quantization error as noise. This concept is only valid for inputs with recurrent crossing of the quantization thresholds and not applicable for example for a DC signal or signals confined into one quantization interval. Successive samples of the quantization error are decorrelated by frequent code transitions, thus spreading the spectrum and making it like a noise [13].

The features of any noise generator are described by two key properties: The

time average power and the noise power spectrum. Where the latter shows how the former spreads over the frequency. For quantization noise, the time average power is contained and the noise power spectrum is meaningful only in the Nyquist interval.

2.2.2.1 Time Average Power

Assuming a uniform probability distribution for the time average power of the quantization error $p(\epsilon_Q)$ in the interval $-\Delta/2 \dots + \Delta/2$ and since the integral of the probability distribution function over the infinite range is equal to one, this results

$$\begin{aligned} p(\epsilon_Q) &= \frac{1}{\Delta} \quad \epsilon_Q \in -\Delta/2 \dots \Delta/2 \\ p(\epsilon_Q) &= 0 \quad \text{otherwise} \end{aligned} \quad (2.7)$$

The time average power of ϵ_Q as expected decreases as the number of bits increases and is given by

$$P_Q = \int_{-\infty}^{\infty} \epsilon_Q^2 \cdot p(\epsilon_Q) d\epsilon_Q = \int_{-\Delta/2}^{\Delta/2} \frac{\epsilon_Q^2}{\Delta} d\epsilon_Q = \frac{\Delta^2}{12}. \quad (2.8)$$

Considering a sine wave as input signal with a maximum amplitude $X_{FS}/2$, its corresponding power is

$$P_{sin} = \frac{1}{T} \int_0^T \frac{X_{FS}^2}{4} \sin^2(2\pi ft) dt = \frac{X_{FS}^2}{8} = \frac{(\Delta \cdot 2^n)^2}{8} \quad (2.9)$$

Eq. 2.8, Eq. 2.9 and Eq. 2.6 lead to the following relation between the maximum achievable SNR and the number of bits of the quantizer for a sinusoidal input.

$$SNR_{sin}|_{dB} = (6.02 \cdot N + 1.78) dB \quad (2.10)$$

The max achievable SNR is also called signal-to-quantization noise ratio (SNRQ). Eq. 2.10 reveals that every added bit of resolution increases the SNR by 6 dB. Accordingly, the power of quantization error decreases by a factor of 4. But since this equation accounts only for quantization noise, a more general form is used to consider all possible noise sources defining the equivalent or the effective number of bits (ENOB) of the ADC

$$ENOB_{sin} = \frac{SNR_{tot}|_{dB} - 1.78}{6.02} \quad (2.11)$$

2.2.2.2 Noise Power Spectrum

The power spectrum represents how the noise power spreads over the Nyquist interval. The power spectrum is the Laplace transform of the auto-correlation function

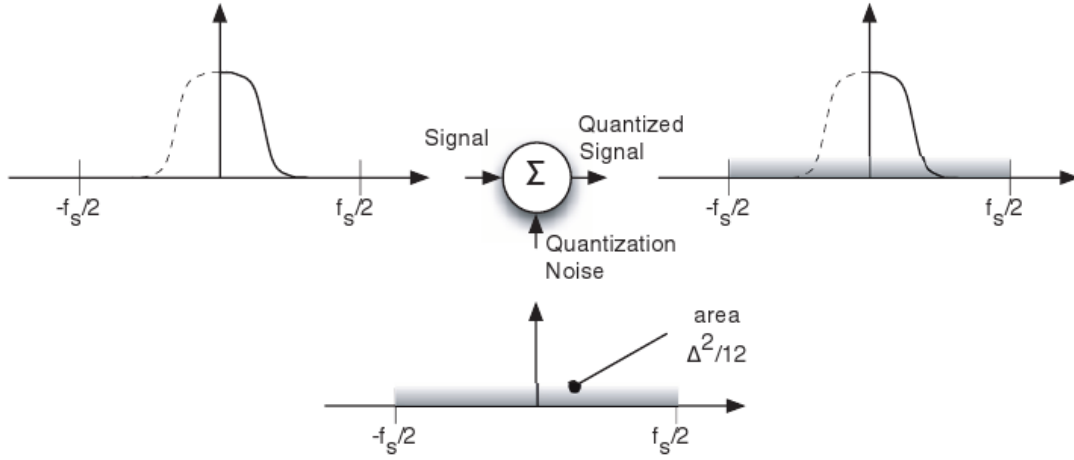


Figure 2.5: Quantization error modeled as an additive white noise

and for sampled data signals it is

$$P_{\epsilon}(f) = \sum_{-\infty}^{\infty} R_{\epsilon}(nT) e^{-j2\pi f nT} \quad (2.12)$$

Based on the assumption that the auto-correlation function $R_{\epsilon}(nT)$ goes rapidly to zero for $|n| > 0$, it becomes a delta in the time domain and the spectrum becomes frequency independent as the Laplace of a delta is a constant. Therefore the power spectral density is considered white with power $P_Q = \Delta^2/12$ which spreads uniformly over the Nyquist bilateral spectrum interval $-f_s/2 \dots f_s/2$. The quantization noise power spectrum is illustrated in Fig. 2.5

$$p_{\epsilon}(f) = \frac{\Delta^2}{12f_s} \quad \text{such that} \quad \int_{-\infty}^{\infty} p_{\epsilon}(f) df = \frac{\Delta^2}{12} \quad (2.13)$$

The oversampling converters like Sigma Delta use a sampling frequency much higher than the signal bandwidth. This technique spreads the quantization noise over a spectrum wider than the signal bandwidth, decreasing the in-band quantization noise and thus increasing SNR.

$$SNR_{sin}|_{dB} = 6.02 \cdot N + 1.78 + 10 \log \left(\frac{f_s}{2f_B} \right) \quad (2.14)$$

2.3 Converter Specifications

A large set of specifications describe the performance of an analog-to-digital converter, the most important are stated and defined in this section.

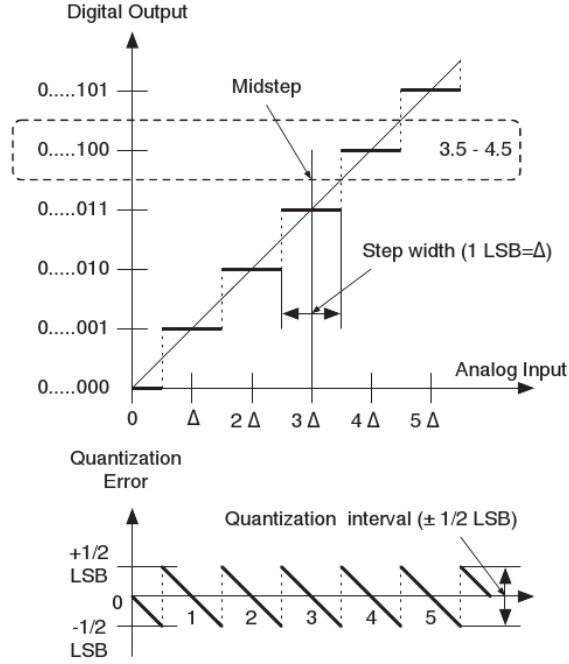


Figure 2.6: Ideal input-output transfer function of an ADC

2.3.1 Static Specifications

The input-output transfer characteristic depicts the static behavior of a data converter so it is the basis for all static specifications. For an ideal case the input-output characteristic is a staircase with uniform steps over the entire dynamic range. Fig. 2.6 plots the initial part of the characteristic for a generic number of bits. If the first and last steps are $\Delta/2$ then the full-scale range is divided by $2^n - 1$ instead of 2^n to give Δ . For this case, where the mid step is representing the quantization interval, the resulting quantization error is shown in Fig. 2.6. It is equal to zero at the mid step and ranges between $\pm\Delta/2$ along the interval.

- **Offset:** The offset describes a shift for zero input. It changes the transfer characteristic so that all the quantization steps are shifted equally as shown in Fig. 2.7 (a).
- **Gain error:** Fig. 2.7 (b) shows this error caused by the deviation of the slope of the straight line interpolating the transfer curve for a data converter from its expected value (ideally 1).
- **DNL:** The Differential Non Linearity is the deviation of the step size of a real data converter from the ideal width of the bins Δ . Assuming that X_k is the transition point between successive codes $k-1$ and k , then the width of the bin k is $\Delta_r(k) = (X_{k+1} - X_k)$. The differential non linearity is

$$DNL(k) = \frac{\Delta_r(k) - \Delta}{\Delta} \quad (2.15)$$

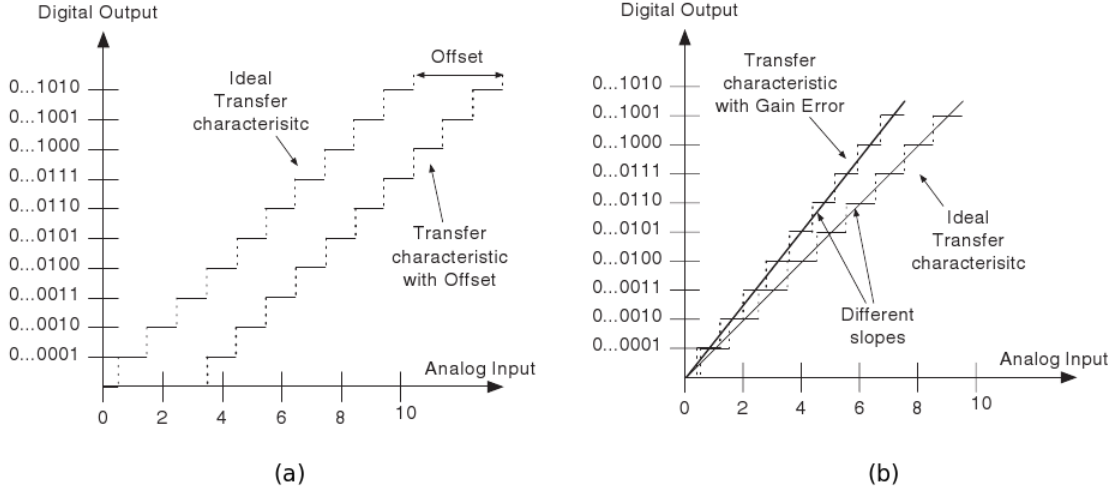


Figure 2.7: Non ideal ADC transfer characteristics due to (a) Offset error (b) gain error

Fig. 2.8 (a) gives an example of DNL error for a possible 12-bit ADC, the error is confined between $\pm\Delta/2$

- **INL:** The Integral Non Linearity is defined as the measure of the deviation of the transfer function from the endpoint-fit line. The use of endpoint-fit line corrects the gain and offset errors. As shown in Fig. 2.8 it corrects the two limits and shows zeros at the two endings of the quantization range INL is very informative in estimating harmonic distortion.

Considering the endpoint-fit line which is the transfer curve with corrected gain and offset. The transition point between codes after correction, $X'(k)$ is given by

$$X'(k) = \Delta'[k_{os} + \sum_{i=1}^k DNL(i)]. \quad (2.16)$$

Where $\Delta' = \Delta(1+G)$; G gain error; k_{os} is the offset measured in LSB. Since the offset compensated for the endpoint-fit line is $k_{os}\Delta'$, the INL in LSB becomes

$$INL(k) = \frac{X'(k) - k\Delta'}{\Delta} = (1+G) \sum_{i=1}^k DNL(i). \quad (2.17)$$

Showing that the INL at bin k is the running sum of the DNL corrected by the gain error. This running sum is added to the quantization and degrades the SNR. A large INL means a large deviation of the transfer curve from the straight line thus causing harmonic distortion.

- **Monotonicity:** This is the ADC feature that produces output codes that are consistently increasing with increasing input signal and consistently decreasing

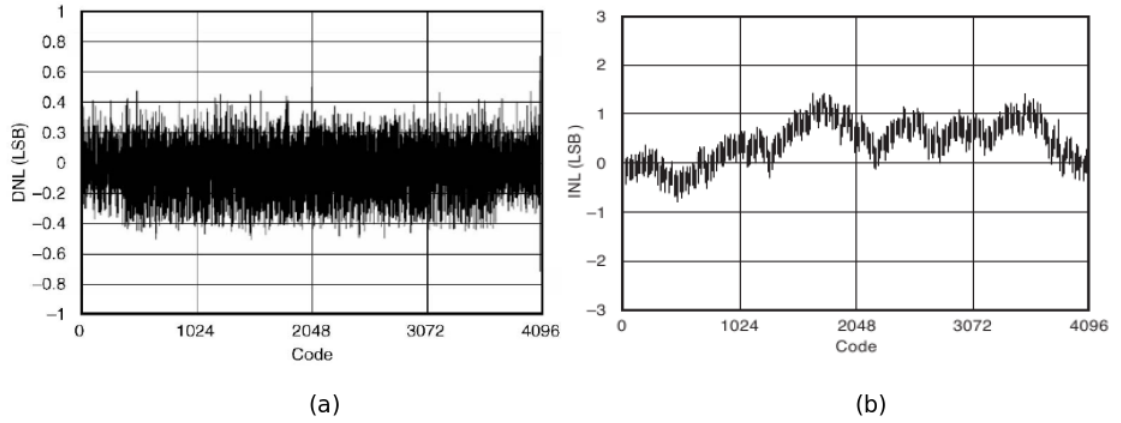


Figure 2.8: Possible 12-bit ADC (a) DNL error (b) INL error obtained with the endpoint-fit line

with decreasing input signal. Therefore the output code will always either remain constant or change in the same direction as the input

- **Missing code:** This denotes when digital codes are skipped or never appear at the ADC output. Since missing codes cannot be reached by any analog input the corresponding quantization interval is zero. Therefore the DNL becomes -1 .
- **Hysteresis:** This is the limit that denotes the dependence of the output code on the direction of the input signal (increasing or decreasing). If this happens, hysteresis is the maximum of such differences.

2.3.2 Dynamic Specifications

The frequency response and speed of the analog components of a data converter determine its dynamic performance. A quality factor of a dynamic feature is its capability to remain unchanged within the entire range of dynamic operation

- **SNR:** The Signal to Noise Ratio is the ratio between the power of the signal (normally a sine wave) and the total noise produced by quantization and the noise of the circuit. The SNR accounts for the noise in the entire Nyquist interval. It may depend on the frequency of the input signal but normally it is constant in the first Nyquist zone and it decreases proportional to the input amplitude. Fig. 2.9 (a) shows the effect of input frequency on the SNR and Fig. 2.9 (b) shows the effect of input amplitude change on the SNR.
- **SNDR:** The signal to noise and distortion ratio is similar in definition to the SNR except that non linear distortion terms, generated by the input sine wave are also accounted for. SNDR is the ratio between the root-mean-square of the signal and the root-sum-square of the harmonic components plus noise excluding DC. Since static and dynamic limitations cause a non-linear response the SNDR depends on both frequency and amplitude of the input sine wave.

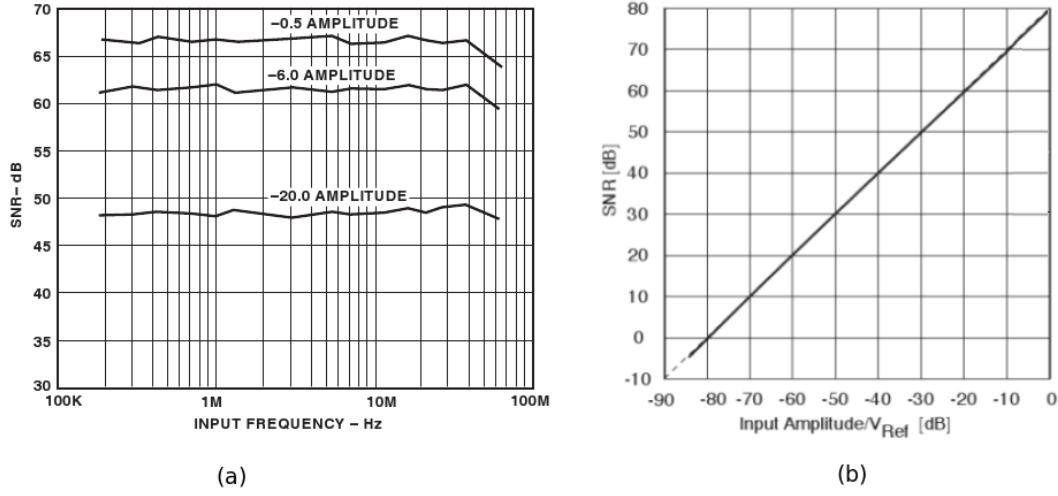


Figure 2.9: SNR degradation for an ADC using sampling frequency of 50MHz with (a) Input frequency (b) Input amplitude

- **DR:** The Dynamic Range is defined as the value of the input signal at which the SNR or SNDR is 0 *dB*
- **SFDR:** The Spurious Free Dynamic Range is the ratio of the root-mean-square signal amplitude to the root-mean-square value of the highest spurious spectral component in the first Nyquist zone. SFDR depends on the signal amplitude, since with large input signals, the highest tone is given by one of the harmonics of the signal. For input amplitudes well below the full scale the distortion caused by the signal becomes negligible and other tones not caused by the input become dominant due to the non-linear nature of the converter.
- **ENOB:** Effective Number Of Bits is taking into account non-idealities to represent the effective resolution the ADC can achieve

$$ENOB = \frac{SNDR|_{dB} - 1.76}{6.02} \quad (2.18)$$

- **ERBW:** Effective Resolution Bandwidth is defined as the analog input frequency at which the SNDR drops by 3 *dB* compared to its low frequency value. It gives the maximum signal bandwidth the converter can handle.
- **Harmonic Distortion:** The ratio between the root-mean-square of the signal and the root-mean-square of harmonic components including aliased terms. Unless otherwise specified the harmonic distortion accounts for the second through tenth harmonics. A fully differential system makes the even harmonics negligible in the first two Nyquist zones.

2.4 Power Efficiency of Nyquist Converters

Figure 2.10 shows the three commonly used Nyquist ADC topologies: Flash, Pipeline, and Successive-Approximation. A first order estimation of power and conversion speed of these conventional topologies is performed to identify the best entry point for further power efficiency improvement.

Traditionally, flash ADCs are favored for high-speed N -bit converters since $2^N - 1$ comparators are utilized to make a fully parallel comparison with the entire quantization levels within one clock cycle. Additional power is dissipated due to the decoding circuits solving sparkle and meta-stability issues as well as thermometer-to-binary code conversion. The total power consumption of a Flash ADC therefore roughly scales exponentially with the converter resolution. In Fig. 2.10, the conversion speed is normalized to one for comparison with other architectures corresponding to the fact that the full conversion is complete within one sample clock cycle. An approach to decrease the exponential dependence of the number of comparators on the number of bits is the use of a pipeline ADC.

Instead of fully parallel comparison, it divides the process into several comparison stages, the number of which is proportional to the number of bits. Therefore, the total number of required comparators is greatly reduced, with only N comparators required for a 1-bit per stage, N -bit pipeline ADC. However, due to the pipeline structure of both analog and digital signal path, inter-stage residue amplification is needed which consumes considerable power and limits high-speed operation. While it is possible to make use of open-loop residue amplification [14], an extra calibration loop is needed, increasing overall complexity and power consumption. Therefore, the total power consumption of a pipeline ADC increases $> N$ while decreasing speed < 1 .

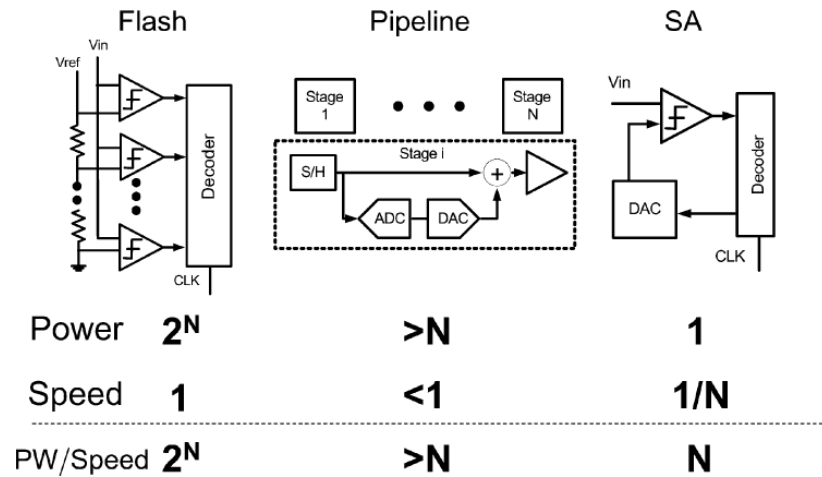


Figure 2.10: Conventional architectures for Nyquist ADCs.

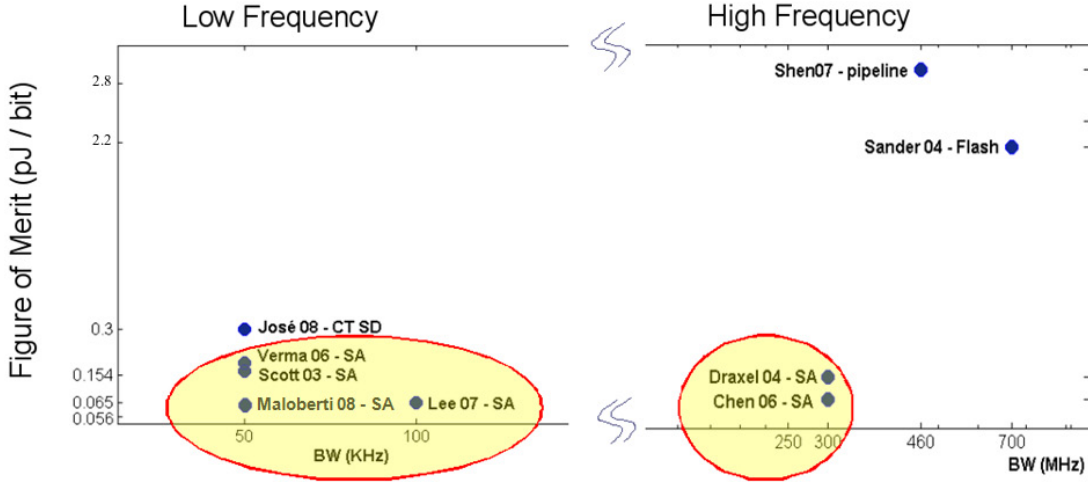


Figure 2.11: The Figure of merit of several architectures of recent realizations of ADC in both low and high frequencies.

For low conversion speeds, the SA approach is often used since it also divides a full conversion into several comparison stages in a way similar to the pipeline ADC, except the algorithm is executed sequentially rather than in parallel as in the pipeline case. An N -bit SA converter utilizes only one comparator with N clock cycles to complete a full conversion. Thus, the total power consumption is normalized to approximately one, while speed is now $1/N$.

Since the ratio of power and speed represents the energy consumption per conversion sample, SA converters clearly have a power efficiency advantage over the other approaches. Due to the fact that the power efficiency difference between SA and Flash topologies increases exponentially with the number of bits N , the SA converter provides a promising starting point for achieving the most power efficient solution. However, the sequential operation of the SA algorithm has traditionally been a limitation in achieving high-speed operation. Architectures based on asynchronous processing, digital calibration and interleaving are reported to yield high-speed operation with a normalized power/speed ratio $\ll N$ [15]-[16].

2.5 State of The Art

A figure of merit FOM is defined to compare performance of different ADCs in terms of power efficiency. It assumes that the total power is consumed mainly because of the bandwidth of the converted signal (BW) and the converter resolution (N)

$$FOM = \frac{P_{Tot}}{2^N \cdot 2 \cdot BW} \quad (2.19)$$

Table 2.1: Performance Summary of Recent Nyquist and Oversampled ADCs implementations.

Reference	Architecture	Tech. (μm)	F_s (MHz)	V_{dd} (V)	ENOB (bit)	ERBW (MHz)	Power (μW)	Area (mm^2)	FOM (pJ/step)
[Maloberti08][17]	SA	0.18	0.1	1.0	9.4	0.05	3.8	0.24	0.056
[Hong07][9]	SA	0.065	0.2	0.9	7.58	0.1	2.47	0.062	0.065
[Verma06][18]	SA	0.18	0.1	1.0	10.55	0.05	25	0.63	0.166
[Scott03][1]	SA	0.25	0.1	1.4	7.9	0.05	4.6	0.053	0.193
[Chen06][16]	SA	0.13	600	1.2	5.30	300	5300	0.12	0.22
[Jose08][19]	Sigma Delta	0.18	3.2	1.2	7.76	0.05	6.6	0.057	0.3
[Draxel04][15]	SA	0.09	600	1.2	5.35	300	10000	NA	0.4
[Sauerbrey03][20]	SA	0.18	0.0041	0.5	6.9	0.002	0.85	0.11	1.186
[Sandner04][21]	Flash	0.13	1200	1.5	5.7	700	160000	0.12	2.2
[Shen07][22]	Pipeline	0.18	800	1.2	5.35	460	105000	0.5	2.8

Where the total power is the power per sample results from dividing the total consumed Energy per sample by the sampling frequency

$$P_{Tot} = E_{Tot} \cdot f_{sampling} \quad (2.20)$$

Sometimes in literature, ERBW replaces BW or the effective number of bits ENOB replaces N changing the expression to

$$FOM = \frac{P_{Tot}}{2^{ENOB} \cdot 2 \cdot ERBW} \quad (2.21)$$

The figure of merit depends on the architecture and the line-width of the technology and it is measured with $\text{pJ}/\text{conv-step}$.

Table 2.1 summarizes the performance of recent state-of-the-art realizations for Nyquist and Oversampled ADCs while Fig. 2.11 sketches their Figure of Merit (FOM) with the Bandwidth (BW). SA-ADC achieves very low power consumption in both low frequency [1]-[9] and high frequency [15]-[16]. The comparison was held between recent realizations of: Continuous-Time Sigma Delta (CT-SD), Successive Approximation (SA), Flash and Pipeline.

2.6 Conclusion

The choice of the successive approximation architecture for applications like wireless sensor nodes was driven by energy considerations; it uses only one comparator independent of the converter resolution, along with a fairly simple switching and logic network to implement the search algorithm. Reconfigurability is offered through cutting down the conversion according to the control logic allowing multiple possible resolutions and less energy consumption. Assuming that the digital logic contributes very little power (a good assumption since the logic is simple), then energy consumption is dominated by two processes: (1) charging the DAC output

to reference voltages and (2) the N comparison operations (where N is the number of bits of resolution desired in the resulting conversion).

Successive Approximation ADC

System Design

3.1 Introduction

This chapter introduces the architecture of a Successive approximation ADC. The background and operation are presented in section 3.2. The system architectures with dedicated sampling block, double-reference and triple-reference implementations are illustrated in section 3.3. In section 3.5, a system ideal model is described in VHDL-AMS and a set of Eldo simulations and MATLAB analysis are made for tabulating the maximum achievable ideal system performance.

3.2 Background and operation

Successive approximation analog-to-digital converters were first introduced in CMOS in the mid-seventies [23]. They lost a lot of interest in the past decade against the Sigma Delta, Pipeline and Flash converters. The research interest in this period was targeting performance in terms of sampling rate and resolution. Later, the successive approximation regained interest after being introduced in high frequency [15] and as a potential candidate for energy constrained systems [2]-[1]. These new applications don't require high resolutions yet demand power efficient ADCs. The current interest in this technique was due to its minimal analog circuitry that allows a direct benefit of the technology scaling in terms of consumption and technology portability.

3.2.1 Flexibility

The successive approximation architecture offers greater flexibility to perform general operations on the input. As shown in Fig. 3.1 (a), it uses only one comparator, along with simple digital logic and a switching network to implement the search algorithm. Assuming a binary search, reduced resolution samples can be obtained by simply ending the search algorithm early. Thus, an N -bit successive approximation ADC can produce outputs ranging from 1 to N bits of resolution with no circuit modifications, using less energy for less resolution.

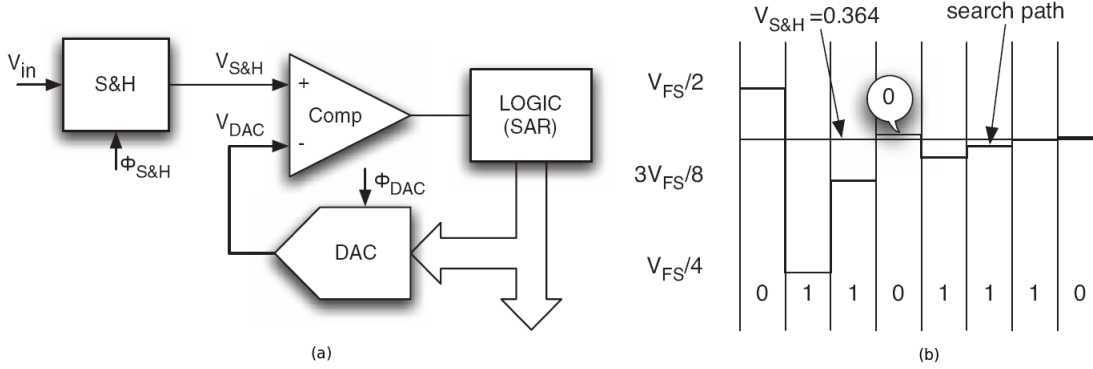


Figure 3.1: (a) Basic block diagram of the successive approximation ADC. (b) An example of a search path

While algorithmic ADCs also provide this feature [24]-[25], the successive approximation architecture offers an additional layer of flexibility through direct modification of the algorithm realized by the successive approximation register (SAR) which could be implemented by a custom microprocessor, and thus can be easily reconfigured. For example, the microprocessor (which now acts as the SAR) could change the search to simply threshold the input, bin the input into an arbitrary number of bins, or start the search at the value of the last output code. By implementing these SAR modes with dedicated hardware in the microprocessor, the energy overhead is minimized. This arbitrary control is programmable by the user at the application level, making the successive approximation ADC extremely flexible.

3.2.2 Principle of Operation

The successive approximation algorithm performs the analog-to-digital conversion over multiple clock periods by exploiting the knowledge of previously determined bits to determine the next significant bit. The method aims to reduce the circuit complexity and power consumption using a low conversion rate by allowing one clock period per bit (plus one for the input sampling).

For a given dynamic range $0 - V_{FS}$ the MSB distinguishes between input signals that are below or above the limit $V_{FS}/2$. Therefore, comparing the sampled input with $V_{FS}/2$ obtains the first bit. The knowledge of the MSB restricts the search for the next bit to either the upper or lower half of the $0 - V_{FS}$ interval. Consequently, the threshold for determining the second bit is either $V_{FS}/4$ or $3V_{FS}/4$. After this, a new threshold is chosen and the next bit can be estimated and the operation goes on till the end of conversion leading to a binary search path. The voltages used for the comparisons are generated by a Digital-to-Analog Converter (DAC) under the control of the logic system known as the successive approximation register (SAR). An example of a search path is shown in Fig. 3.1 (a).

The operation needs one clock period for the sample-and-hold (SH) and one clock period for the determination of every bit thus requiring $(N + 1)$ clock intervals for an N -bit conversion. Sometimes, if the SH settling period is significantly longer than the time required for each comparison, then it can be convenient to use two clock periods for the sampling and one per every bit totaling $(N + 2)$ clock intervals for an N -bit conversion. Note that the SAR control is such that V_{DAC} tracks V_{SH} thus establishing a search path. Fig. 3.1 (b) shows an example of search path for $V_{SH} = 0.364 V_{FS}$. The name of the algorithm comes from the fact that the voltage V_{DAC} is an improving approximation of V_{SH} . In every step, the error can be occasionally larger than the previous one but surely is not larger than successive divisions of two of the full-scale amplitude [13].

3.2.3 Conversion Example

An example of 4 bit conversion for the system level architecture described in Fig. 3.1 (a) is showed in Fig. 3.2 . The first clock cycle is reserved for sampling, then the bit checking start at the next clock cycle. The SAR sets the MSB to '1' as a prediction of the MSB value. According to this, the DAC is set to generate $V_{ref}/2$. The sampled signal is larger than $V_{ref}/2$. The comparator confirms the MSB prediction and its value is retained and the $V_{ref}/2$ component is confirmed as a part of the signal.

With the next search interval defined, the next MSB is set to '1', the SAR instructs the DAC to increase its output adding the $V_{ref}/4$ component and the second comparison is held with the sampled signal. Again, the signal is higher, thus $V_{ref}/4$ component is confirmed as a part of the signal and the next MSB value is retained. The operation continues in the same manner, predicting each successive bit until all 4-bits are determined. The analog signal is finally represented by the digital bits filling the coefficients of the following equation:

$$V_{in} = b_1 \frac{V_{ref}}{2^1} + b_2 \frac{V_{ref}}{2^2} + b_3 \frac{V_{ref}}{2^3} + b_4 \frac{V_{ref}}{2^4} \quad (3.1)$$

The Digital codes representations is selected such that analog levels less than $V_{ref}/16$ are mapped to the code '0000', those levels above $15V_{ref}/16$ are mapped to the code '1111' and so on for the other ranges in between.

3.3 System Architecture

The main concept of capacitive DACs relies on the fact that the series of two capacitors, initially discharged and connected between V_{ref} and ground, yield in the steady state a middle point voltage. Fig. 3.3 (a) shows the resulting capacitive divider.

$$V_{out} = V_{ref} \frac{C_1}{C_1 + C_2} \quad (3.2)$$

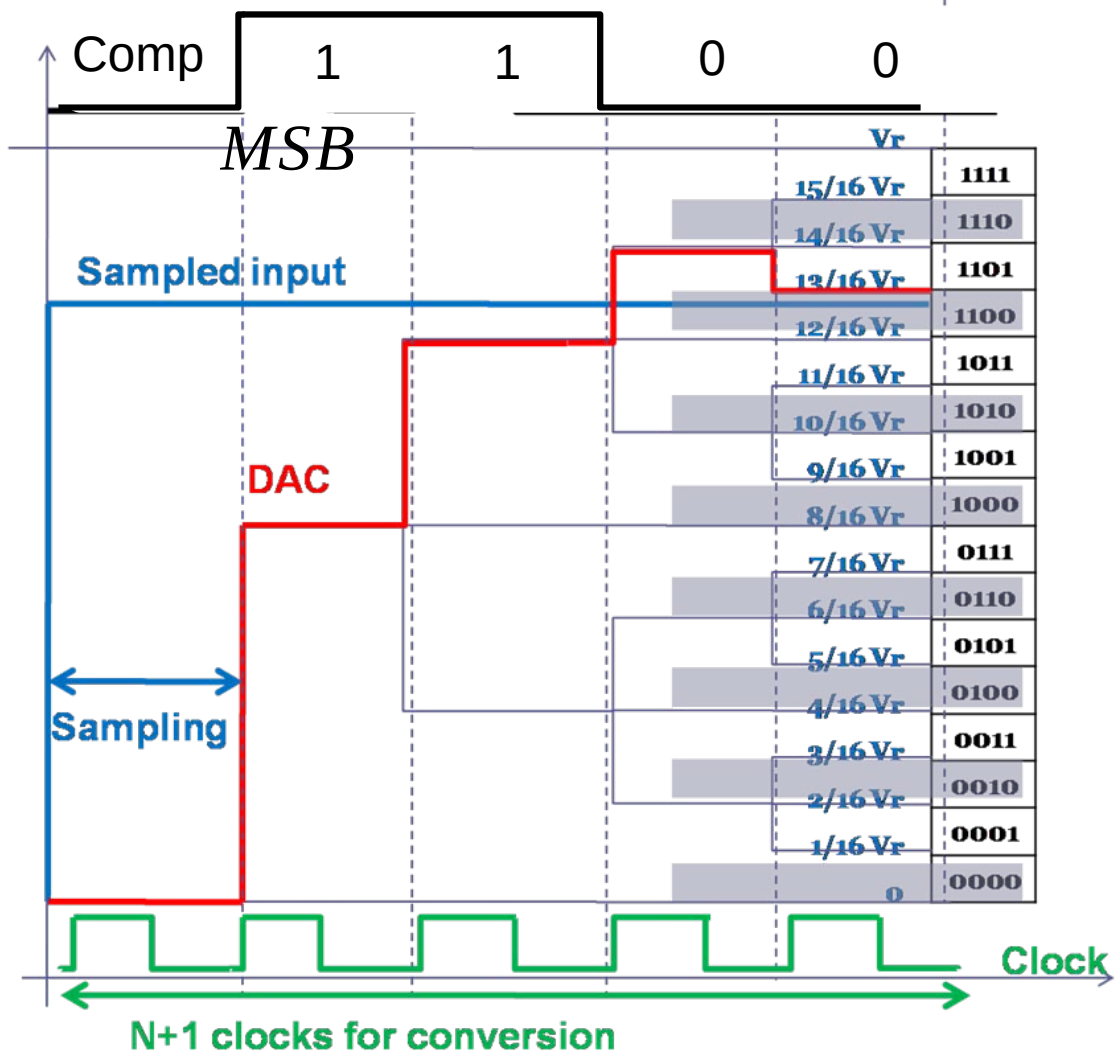


Figure 3.2: An Example of 4 bit conversion: clock, comparator output, DAC output, analog sampled input, digital output, all possible search paths and the digital codes mapping

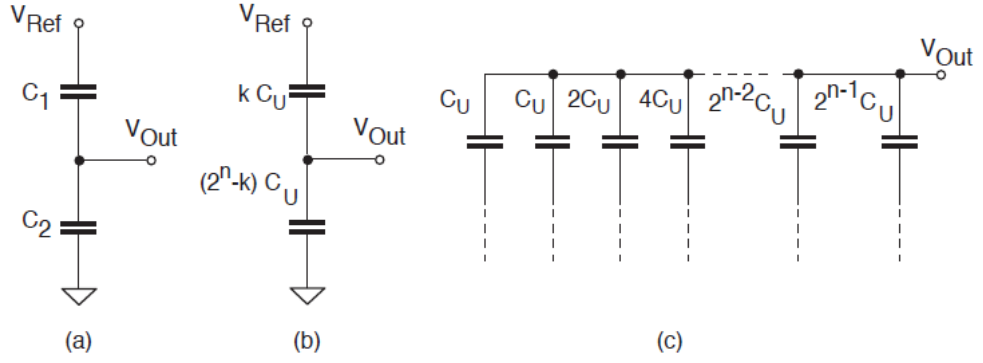


Figure 3.3: (a) and (b) Simple capacitor divider. (c) Array of binary weighted capacitors.

Fig. 3.3 (b) presents the equivalent of an arbitrary arrangement for a 2^n capacitors DAC while Fig. 3.3 (c) shows their initial arrangement. The capacitors used are multiples of a unity element (C_U) and have total value $2^n C_U$. C_1 is made by k unity elements and C_2 is the rest of the 2^n thus leading to a voltage equal to $V_{out}=V_{ref}$. $k/2^n$ as required by a DAC. Often, the two capacitors make an array of binary weighted elements (C_U , C_U , $2C_U$, $4C_U$, ..., $2^{n-1}C_U$) that sums up $2^n C_U$ as shown in Fig. 3.3 (c). The combination of the elements realizes the two capacitors by connecting the bottom terminals to ground or to V_{ref} depending on the binary combination required to obtain k . With the full-scale voltage defined as $2^{n-1}V_{ref}/2^n$, the one unity capacitance is always connected to ground.

3.3.1 Dedicated Sampling Block

The first possible architecture is to use a dedicated sample-and-hold block directly connected to the first comparator terminal and to use the DAC on the other comparator terminal as illustrated in Fig. 3.4. The full conversion is preceded by a reset phase ϕ_R during which the array is discharged by setting all the switches such that the bottom plates are grounded. During conversion phase the reset switch opens and the bottom plates of the binary weighted capacitors are connected to V_{Ref} or ground according to the value of the control bits. After each clock switches change position to increase or decrease the DAC output following the signal.

The input capacitance of the comparator is in parallel with the parasitic capacitance of the array, thereby it must be considered in order to keep the gain error and the harmonic distortion as low as possible.

This architecture is suitable for single-ended or pseudo-differential implementations. For differential versions, the sampling is made by the DAC itself through the

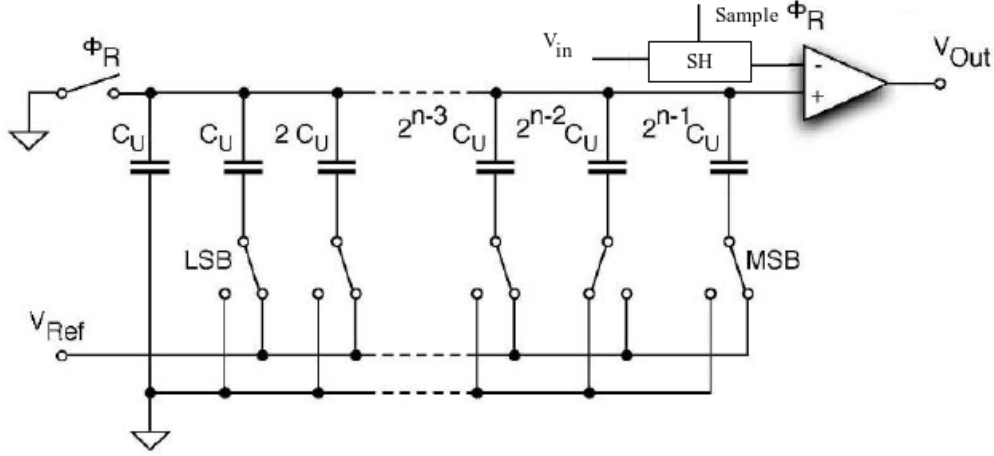


Figure 3.4: System architecture with dedicated sampling block

classic charge redistribution scheme [23]-[26]-[27]. It is better to use this architecture at reduced supply voltages to guarantee the linearity of the sampling process with minimal circuit complexity. Sampling using all the DAC capacitors at very low voltages needs 2^N special low-voltage switches [28] that will increase the consumed power and area.

A drawback of the direct implementation of capacitive divider architectures is that the number of elements increases exponentially with the number of bits. Since technological limits and matching requirements determine the minimum size of the unity capacitance, an increase in the number of elements augments the total capacitance and, in turn, increases the silicon area and the power required for the voltage reference generator.

3.3.2 Double-Reference Charge Redistribution

The different phases of operation for the 4 bit SA example described in section 3.2.3 using the binary weighted capacitive divider DAC with the classical charge redistribution mechanism [26] is shown in Fig. 3.3.2 (a). The DAC in this architecture also performs the sampling and thus eliminates the need for a dedicated sample-and-hold circuit and consequently reduces the power consumption and area. Leaving only one critical analog active block in the design which is the comparator.

The conversion starts at the rising of the sampling signal. The upper plates of all capacitors are switched to V_{ref} while the bottom plates switches are connected to the analog input signal yielding a sampled value of $V_{ref} - V_{in}$ across the binary weighted capacitor array. Next, the invert signal connects the bottom plates of all capacitors to the ground. For conservation of charge the upper plates voltage jumps

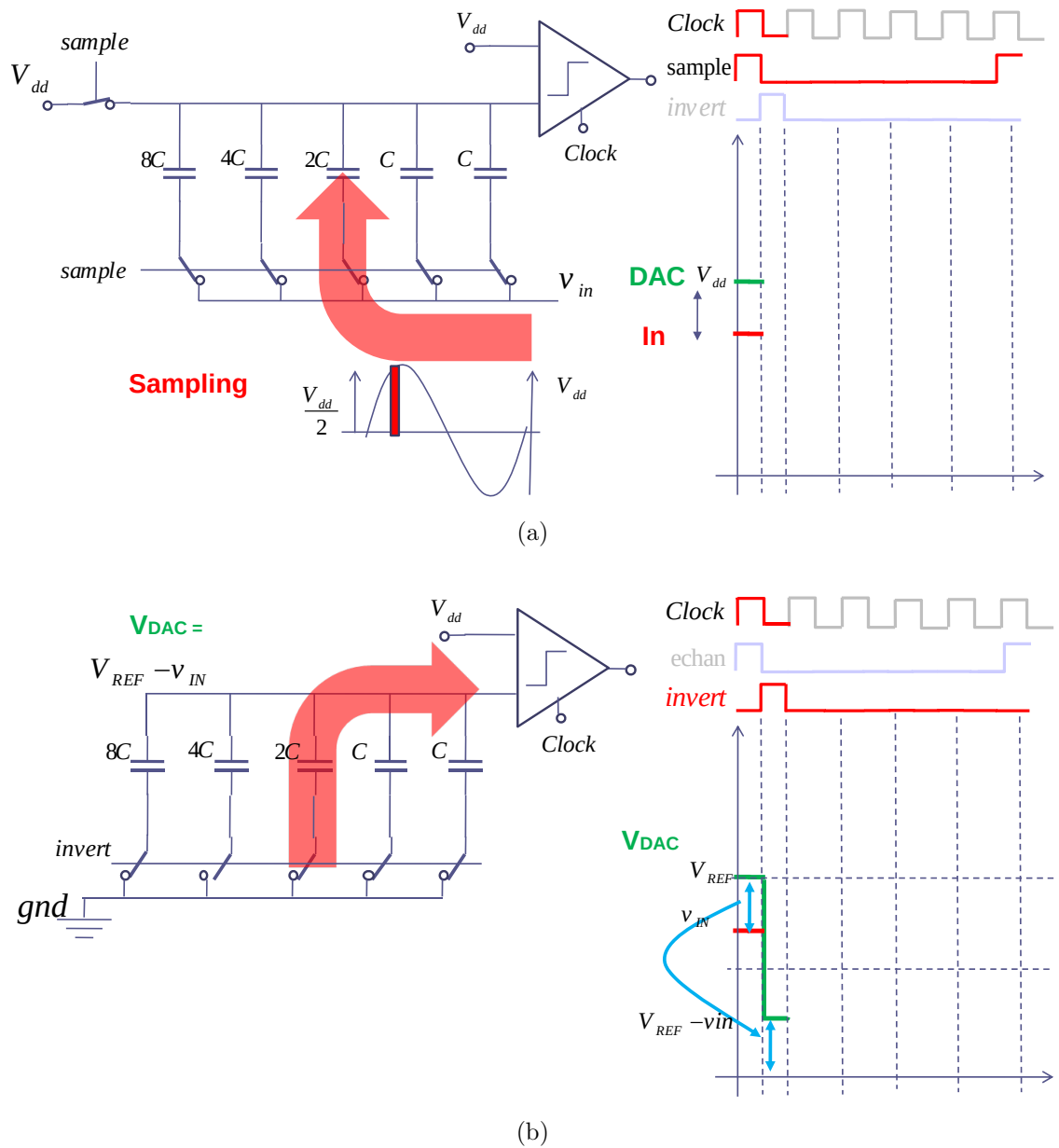


Figure 3.5: Single-Ended Operation with Double Reference (a) Sampling phase (b) Inverting phase

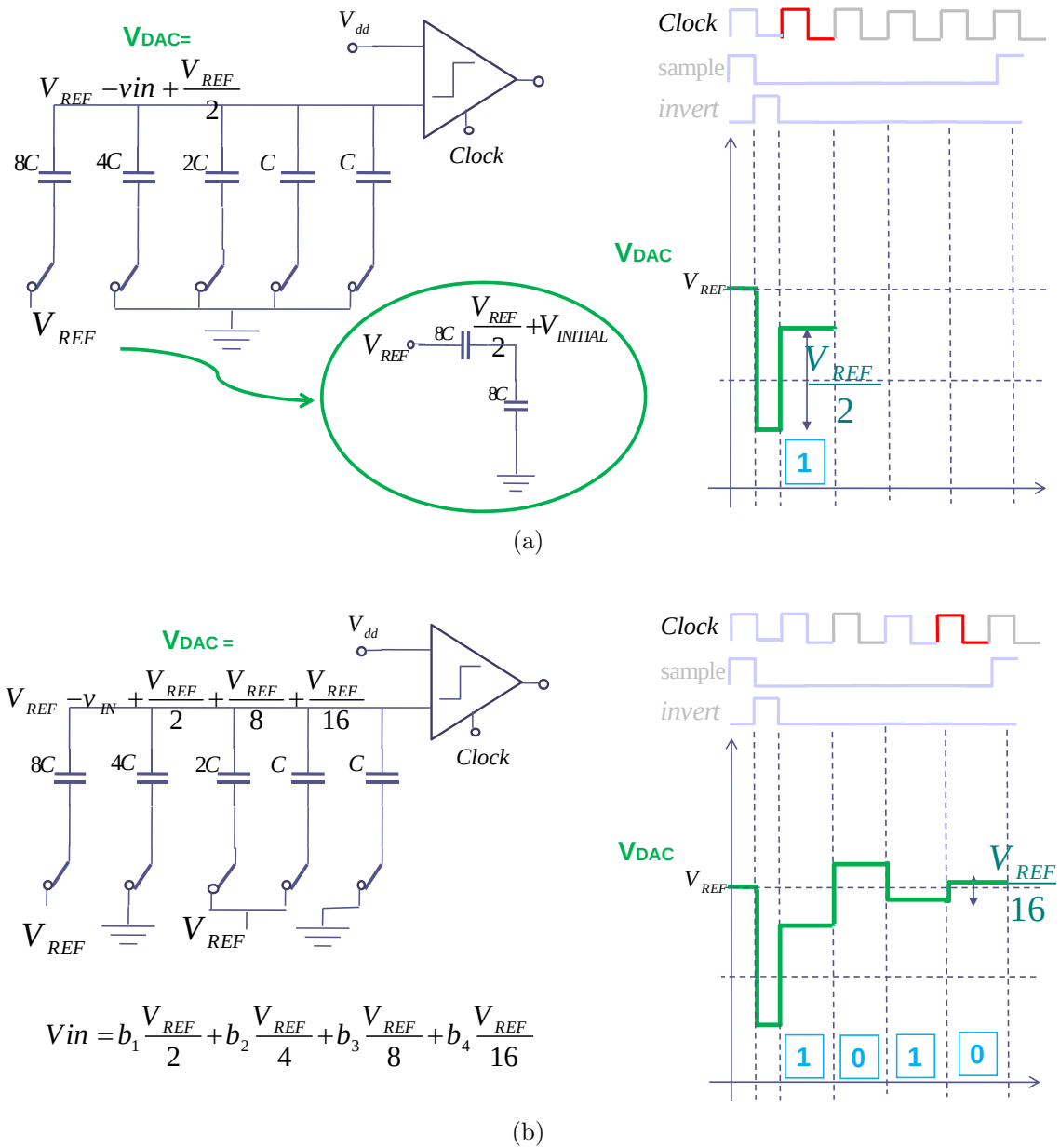


Figure 3.6: Single-Ended Operation with Double Reference (a) Charge redistribution phase to find the MSB (b) The final switches arrangement after the end of conversion

to $V_{ref} - V_{in}$ and the total sampled charge is now stored on the top plates. The charge redistribution phase starts by testing the value of the MSB. This is done by raising the bottom plate of the largest capacitor $8C$ to the reference voltage V_{ref} . The equivalent circuit is now actually a voltage divider between two equivalent capacitances and the voltage on the upper plates V_{DAC} is increased by $V_{ref}/2$.

$$V_{DAC} = V_{ref} \frac{8C}{8C + 8C} + V_{initial} = \frac{V_{ref}}{2} + V_{ref} - V_{in} \quad (3.3)$$

The next SAR step is to add or subtract $V_{ref}/4$ according to the comparison result of V_{DAC} with V_{ref} . In both cases, the $4C$ capacitor bottom plate is switched to V_{ref} . Then, if it is an addition, the $8C$ capacitor is kept connected to V_{ref} else it is switched back to ground removing its voltage component $V_{ref}/2$. In Fig. 3.3.2 (a) the comparator detects that $V_{DAC} < V_{ref}$, so the $8C$ capacitor is kept in position and the $4C$ capacitor is switched to V_{ref} . The resulting voltage increment comes from the voltage division between $4C$ and $12C$ such that V_{DAC} increases by $V_{ref}/4$

$$V_{DAC} = V_{ref} \frac{4C}{12C + 4C} + V_{initial} = \frac{V_{ref}}{4} + \frac{V_{ref}}{2} + V_{ref} - V_{in} \quad (3.4)$$

So, at the k SAR cycle, an addition corresponds to raising the bottom plate of the k capacitor to V_{ref} . A subtraction corresponds to raising the bottom plate of the k capacitor to V_{ref} and turning back the bottom plate of the $k-1$ capacitor to ground. The final switches arrangement is shown in Fig. 3.3.2 (b). Only the capacitors of the corresponding binary weights to form the sampled analog signal are holding the charge while the others are discharged.

$$V_{DAC} = V_{ref} - V_{in} + \frac{V_{ref}}{2} + \frac{V_{ref}}{8} + \frac{V_{ref}}{16} \quad (3.5)$$

With $V_{DAC} \approx V_{ref}$ at the end of conversion, and the signal is reconstructed at the form of Eq. 3.1

$$V_{in} = \frac{V_{ref}}{2} + \frac{V_{ref}}{8} + \frac{V_{ref}}{16} \quad (3.6)$$

Filling the coefficients of Eq. 3.1 with the present components coefficients equal '1' and the absent component coefficients equal '0' gives the digital output '1010'.

3.3.3 Leakage Problem

Usually in modern technologies with the continuous decrease in the supply voltage it's preferred to use $V_{ref} = V_{dd}$ to increase the dynamic range. Because of this, one important point to consider is that during the conversion, sometimes $V_{DAC} > V_{dd}$ for a maximum worst case of $V_{DAC} = 1.5V_{dd}$ corresponding to a zero input signal level.

The switch used in the sampling phase which connects the DAC output to V_{ref} which appears in Fig. 3.3.2 (a) is usually implemented with a simple PMOS tran-

sistor. With the low-threshold voltages of the current technologies, leakage of the charge stored in the capacitor array may happen through this switch. The use of a boosted clock to force a strong OFF switch state cannot be employed anymore due to the gate dielectric reliability limitation in advanced low-voltage CMOS processes.

To solve this leakage problem without clock boosting techniques, the special charge-pump switch proposed in [1] or a low-voltage bootstrapped switch [28] can be used to beat this problem with adequate reliability.

3.3.4 Triple-Reference Charge Redistribution

For differential implementation, as previously explained, no dedicated sampling block may be used and the sampling is done through the DACs. Double-reference charge redistribution may be used for each DAC. The output of the converter will follow the signal of only one DAC. The second DAC signals are the complement of their counterpart in the first one. The use of binary weighted capacitors in a differential double-reference implementation will double the input sampling capacitance.

The total capacitance may be cut down to half through the use of a triple-reference architecture allowing addition and subtraction by switching only one capacitor per cycle. Switching only one capacitor per bit-cycling step decreases the

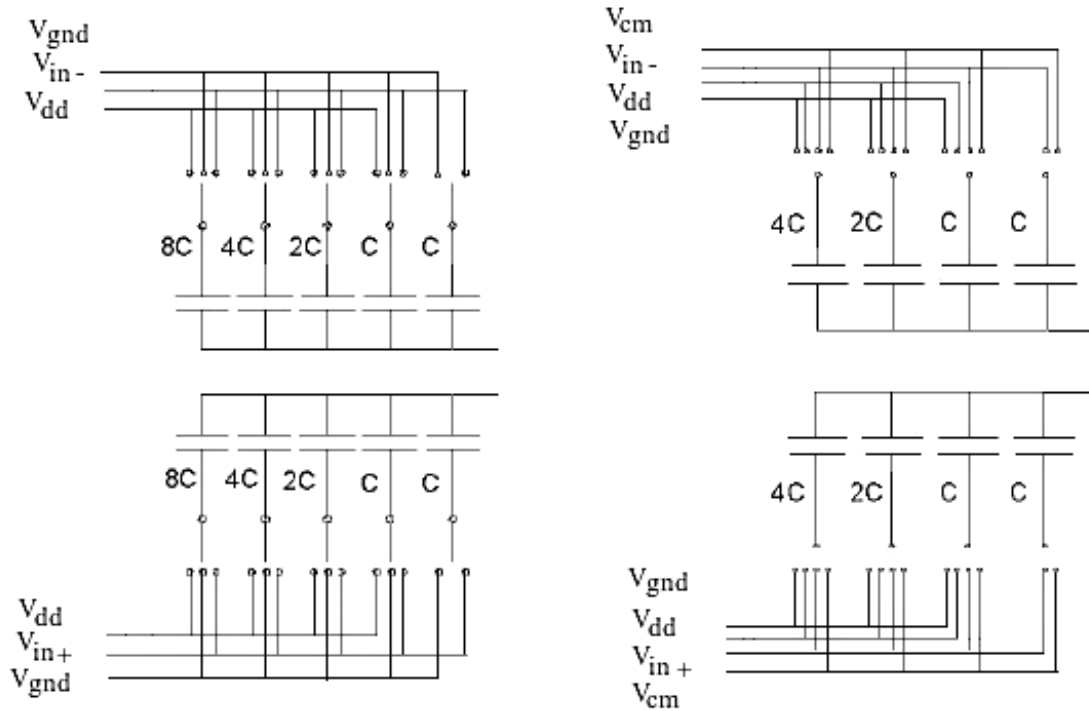


Figure 3.7: 4 bit Differential DAC (a) double reference (b) triple reference.

power consumed in the DACs [29]. Both different architectures are presented using binary weighted conventional DACs in Fig. 3.7. The architecture of Fig. 3.7 (a) works exactly like the single-ended double-reference version illustrated in the previous section typically operating with V_{dd} and V_{gnd} .

The version shown in Fig. 3.7 (b) uses 3 reference voltages: V_{dd} , V_{cm} and V_{gnd} . It allows adding and subtracting by switching only one capacitor each time regardless of the comparator output. Moving the largest capacitor from V_{cm} to V_{dd} corresponds to an addition, while moving it to V_{gnd} corresponds to a subtraction. Very-low-voltage applications may demand special switches in sampling to guarantee rail-to-rail operation. This is why Sampling through the upper plates, shown in Fig. 3.7, is sometimes favored to minimize the number of these switches.

The operation of the DAC of Fig. 3.7 (b) will be illustrated since it is the most common for differential implementations. A differential architecture implementation of the 4 bit SA is shown in Fig. 3.3.4. The sampling operation is the same but the upper plates are connected to $V_{dd}/2$ rather than V_{dd} . The lower and upper capacitor arrays are charged to $V_{dd}/2 + V_{in}/2$ and $V_{dd}/2 - V_{in}/2$ respectively by the end of the sampling phase.

Fig. 3.3.4 (b) shows the inversion phase; the bottom plates of all capacitors are connected to $V_{dd}/2$ so that the upper plate voltage in the lower DAC output jumps to $V_{dd}/2 - V_{in}/2$ while the upper DAC output becomes $V_{dd}/2 + V_{in}/2$.

The charge redistribution phase starts in a different way than that of the single-ended version. The first comparison is held just after the inversion to decide whether to add or subtract the $V_{dd}/2$ component.

As shown in the differential DACs output signals of Fig. 3.3.4 (b), the signal $V_{dd}/2 + V_{in}/2 > V_{dd}/2 - V_{in}/2$ so $DAC2 > DAC1$. For returning back to the initial voltage $V_{dd}/2$, DAC1 has to increase and DAC2 has to decrease. Notice that switching the largest capacitor 4C bottom plate from $V_{dd}/2$ to V_{dd} will increase DAC1 by only $V_{dd}/4$. This movement implies a complementary movement in DAC2 switching 4C from $V_{dd}/2$ to ground and the differential resulting increment is equivalent to $V_{dd}/2$. Again the comparisons and the capacitor switching continue till the final settlement of the switches is reached in Fig. 3.3.4 (b) and the conversion ends with the same result '1010'.

This triple-reference differential architecture needs a reference generation for $V_{dd}/2$. In terms of components it needs nearly six times the number of switches used in the single-ended double-reference architecture and about double the number of capacitors of a single-ended triple-reference version. The added components and reference voltage will consume more power but it benefits of differential implementations advantages such as better rejection for common mode and power supply noise and even harmonics cancellation. This architecture is recommended for use in high frequencies and besides it does not need any additional special switches.

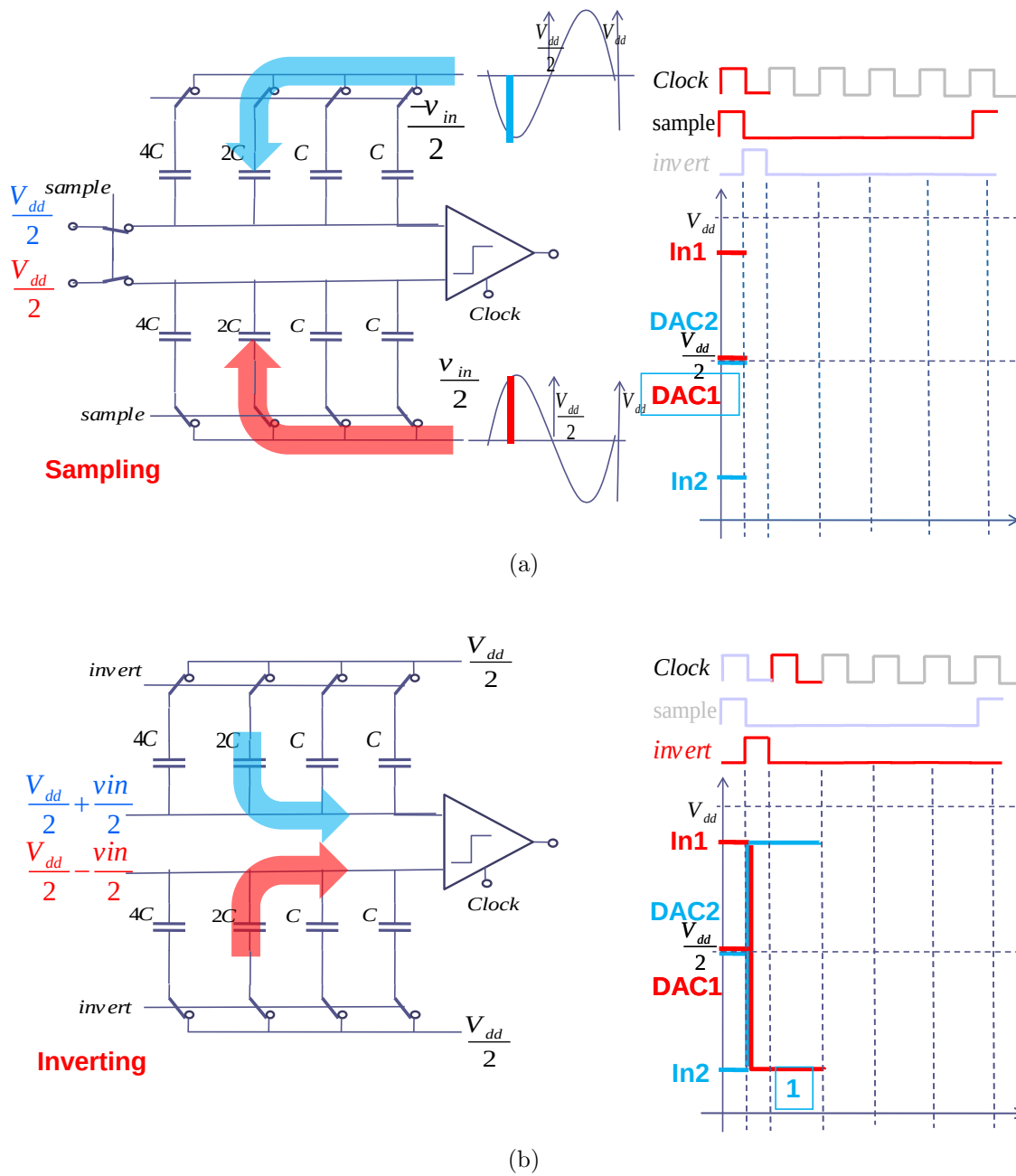


Figure 3.8: Differential operation with triple reference (a) Sampling (b) Inverting and MSB

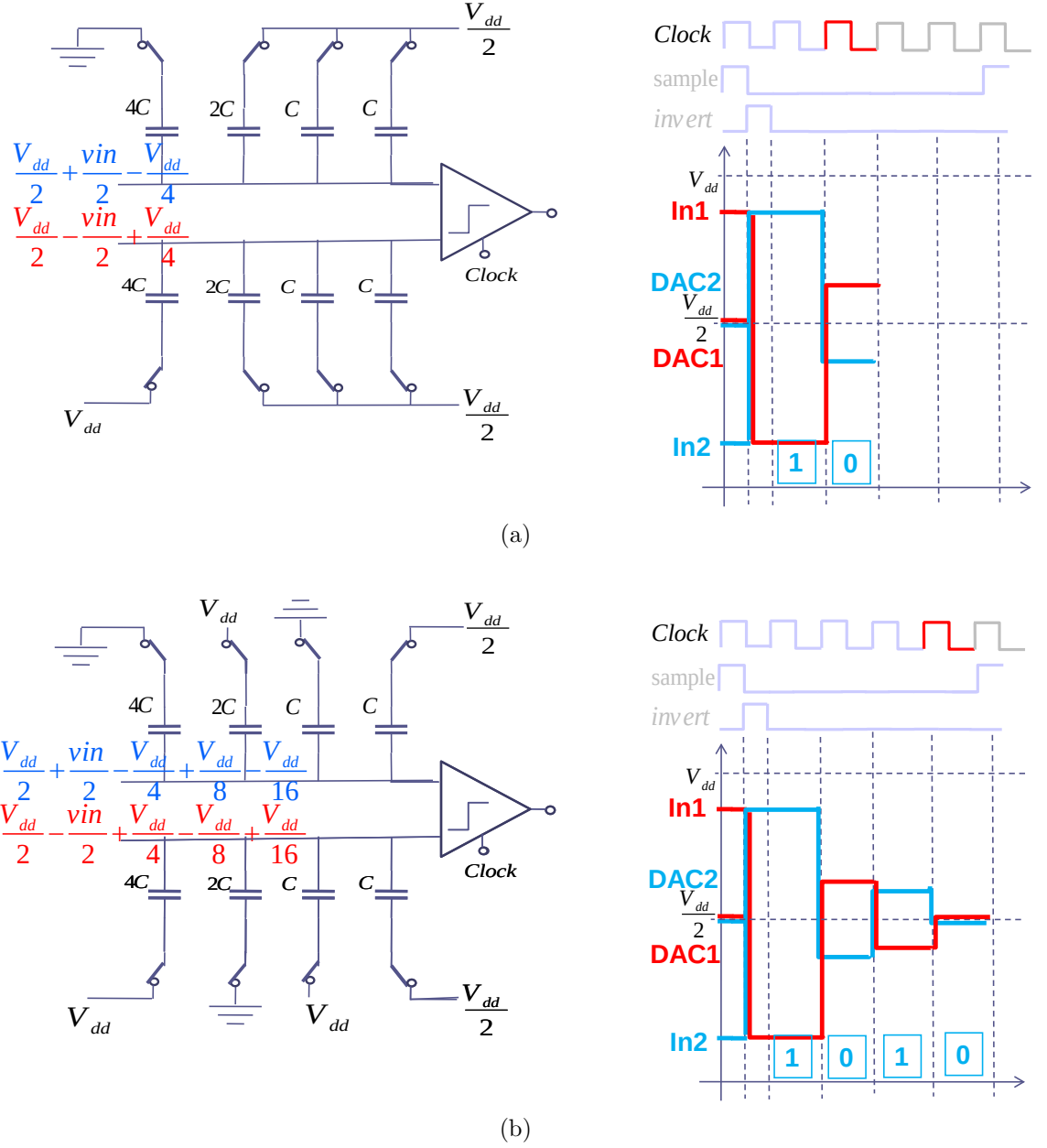


Figure 3.9: Differential operation with triple reference (a) Charge redistribution phase to find the MSB-1 (b) The final switches arrangement and the end of conversion

The single-ended version is usually preferred in low-frequency applications with very-low-power demands such as the wireless sensor nodes [1] or very-low-voltage operation [9]. This will be on the expense of lower noise immunity, power supply noise rejection and harmonics rejection.

3.4 Arbitrary Search

During Conversion, errors may occur due to comparator resolution, settling time and DAC non-linearity. These errors are insignificant if the resulting differences are below $V_{LSB}/2$ and the digital code is not changed. In case the resulting errors are more than $V_{LSB}/2$, conversion error of one to many LSBs occur.

An arbitrary search mode for the SA-ADC allows to start searching from the last converted value using the final arrangement of switches of the last conversion in the start of the new conversion. This way, the last lengthy comparison between the most close values, is obligatory pushed to be the last one. Pushing the comparison operation where both comparator inputs are very close to be the last one will decrease the error possibility to its minimum. Systems with self-timed comparators [30]-[16]-[31] will also benefit leaving the maximum time for the last comparison ensuring enough settling time.

3.5 Behavioral SA-ADC Model

Performance of the ideal SA-ADC is evaluated through a set of transient and frequency analysis followed by sketching the SNR with the normalized input amplitude in dB then with the input frequency. The SAR algorithm for a double-reference single-ended architecture is shown in Fig. 3.10 while that for a triple-reference differential architecture is presented Fig.3.11.

Both presented algorithms were described in VHDL. Analog components like switches, capacitors and comparator were described using ideal ELDO macro-models. VHDL-AMS descriptions were used to interface all blocks allowing mixed system simulation. The time domain analysis results were extracted and processed by dedicated MATLAB programs and bash shell scripts written for the frequency analysis and for tracing the performance curves.

3.5.1 Single-Ended Double-Reference SAR Algorithm

The first step of the single-ended algorithm is to check of the state of the start signal at *clock1* rising edges. With the start signal on, sampling switches are turned on

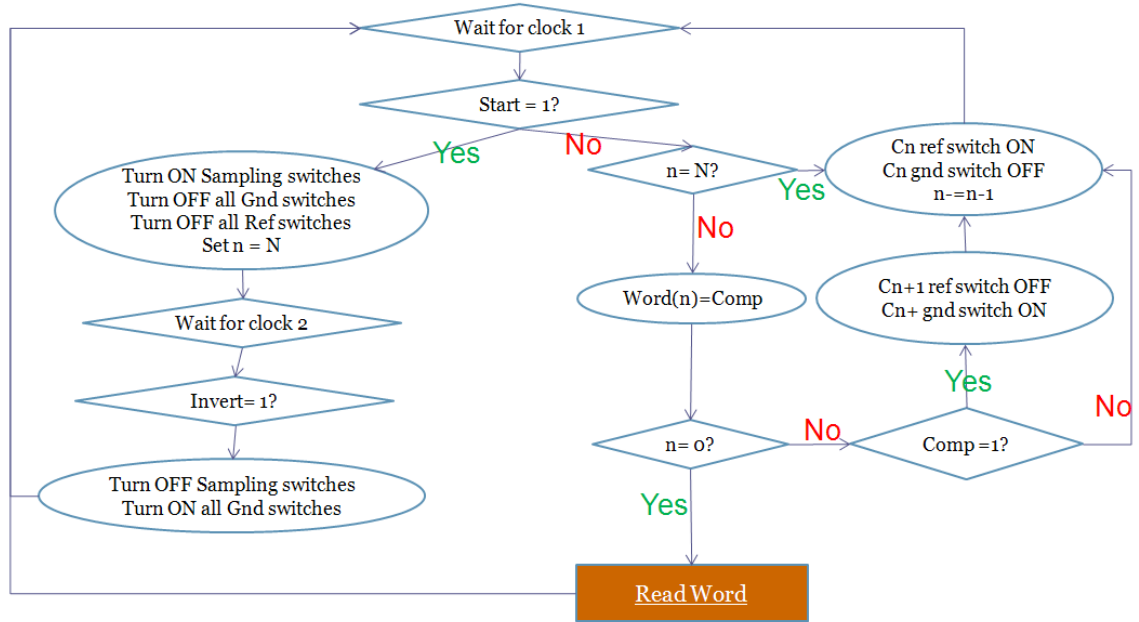


Figure 3.10: SAR algorithm flowchart for a single-ended implementation.

while all ground and reference switches of the DAC are turned off and the counter is set to N . At the rising edge of *clock2*, the invert signal is checked and accordingly the sampling switches are turned off while the ground (inversion) switches are turned on.

The check returns to *clock1* rising edges. While the start signal is off, the counter is checked. For the counter value N which corresponds to the state just after inversion, no comparison checks are needed. The next step is switching on the reference switch of C_N , decreasing the counter value and returning to the *clock1* check. At the next cycles for $0 < n < N$, $word(n) = comp(n)$. Then, the comparator value is checked. For $comp(n) = 1$, C_{n+1} is switched to ground, else it is kept in position. Next C_n is switched to reference, the counter is decreased and the next state is *clock1* check. For $n = 0$, the last comparison result is read without further capacitor switching and the final word is read.

3.5.2 Differential Triple-Reference SAR Algorithm

The first step of the differential algorithm is also to check the start signal state at the rising edges of *clock1*. With the start signal on, the global system reset occurs. The counter is restarted to N , the sampling switches are turned on and all other reference switches are disconnected. At the rising of *clock2*, the invert signal is checked then accordingly the common mode (inversion) switches are turned on and the sampling switches are disconnected.

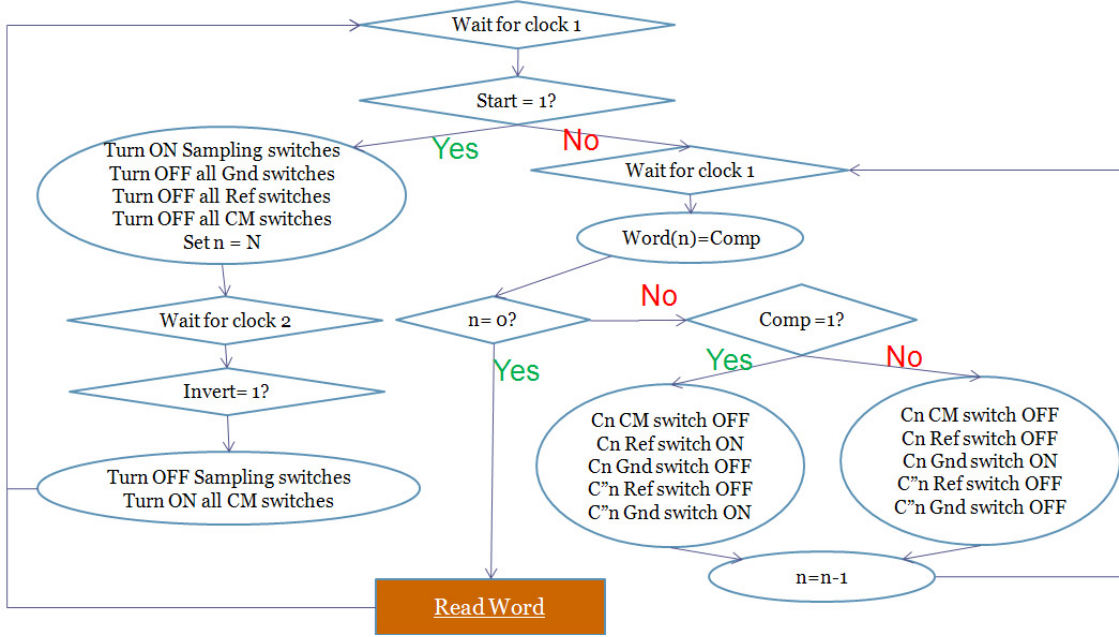


Figure 3.11: SAR algorithm flowchart for a differential implementation.

The check continues for rising edges of *clock1*. The start signal is off and a recommended wait for one more clock is needed in order that the DAC and the comparator have enough settling time. At the next cycles for $0 < n$, $word(n) = comp(n)$, C_n capacitor is disconnected from common mode then the comparator value is checked. For $comp(n) = 1$, C_n is switched to reference else, it is switched to ground. Its complement C'_n is oppositely switched either to reference or to ground. The counter is decreased and the next state is to wait for *clock1* rising edge. When $n = 0$, the digital word is directly read with no more switching and the system waits for the next start signal.

3.5.3 Behavioral Simulations Results

Behavioral descriptions doesn't show differences between differential and single-ended implementations without introducing non-idealities. Static analysis are insignificant with full ideal models since INL and DNL evaluation equal zero for all code values. Only dynamic performance is evaluated in the following set of simulations.

The main system design parameters are the ADC resolution (N) and the clock frequency (f_{clk}) selected according to the system SNR_{max} and bandwidth requirements.

$$DR = SNR_{max} = 6.02N + 1.76dB \quad (3.7)$$

Table 3.1: SNR and clock frequency for different ideal SA-ADC.

Resolution	BW	f_{clk}	SNR_{Calc}	SNR_{Sim}
4 bit	50 KHz	0.5 MHz	25.84	23.21
6 bit	71 KHz	1 MHz	37.88	35.91
8 bit	55 KHz	1 MHz	49.92	47.76

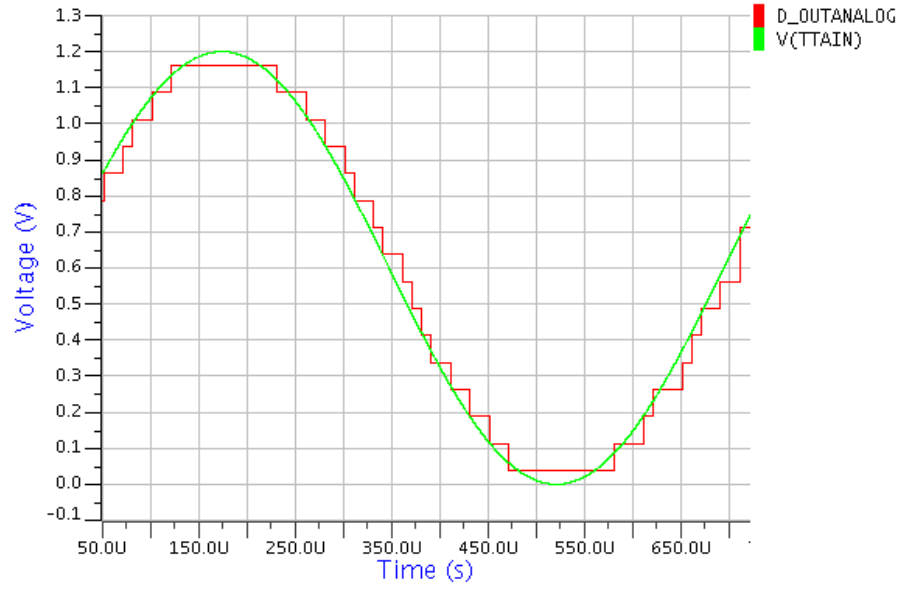


Figure 3.12: Transient response for a 4 bit ideal SA-ADC with a 1.4KHz full-scale sinusoidal and its corresponding digital output in decimal representation.

Where DR is the Dynamic range. The SNR for any input amplitude (A_{in}) can be written in terms of the full-scale input amplitude (A_{FS}) and the DR

$$SNR = DR - 10 \log \left[\frac{A_{in}}{A_{FS}} \right] \quad (3.8)$$

$$f_{clk} = (N + 1)f_s \quad (3.9)$$

Using Eq. 3.7 and Eq. 3.9 with the fact that this is a Nyquist converter, the system design parameters are calculated in Table 3.1 for multiple ADC resolutions. The difference between the simulated SNR values and those calculated from Eq. 3.7 is $\approx 2dB$ due to the selection of a moderate number of points in simulations to have a reasonable simulation time and the same simulation resolution for all description levels. In consequence SNR calculations based on the FFT do not have enough points. The noise floor, represented in these simulations by the quantization noise is a little higher than the theoretical prediction.

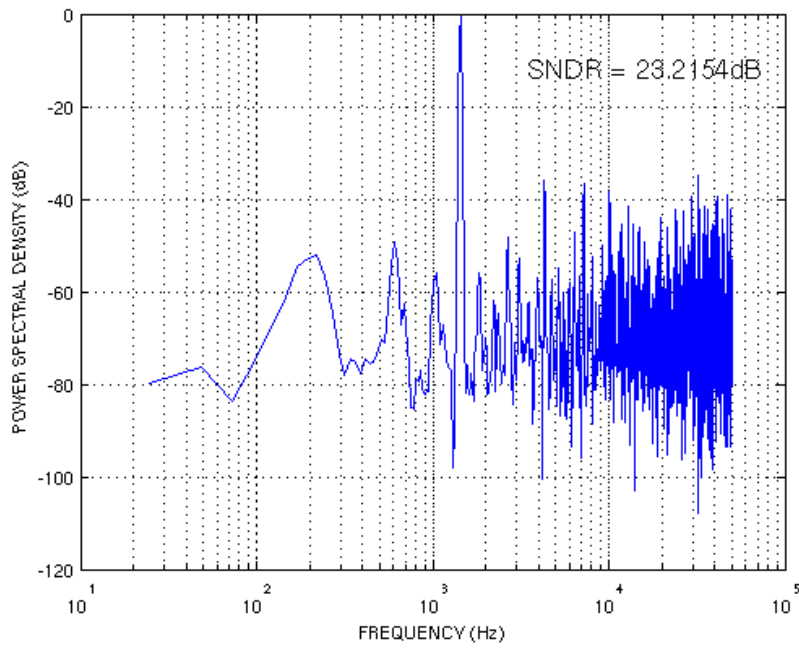


Figure 3.13: Output Spectrum FFT in 4096 points for a 4 bit ideal SA-ADC with a 1.4KHz full-scale sinusoidal

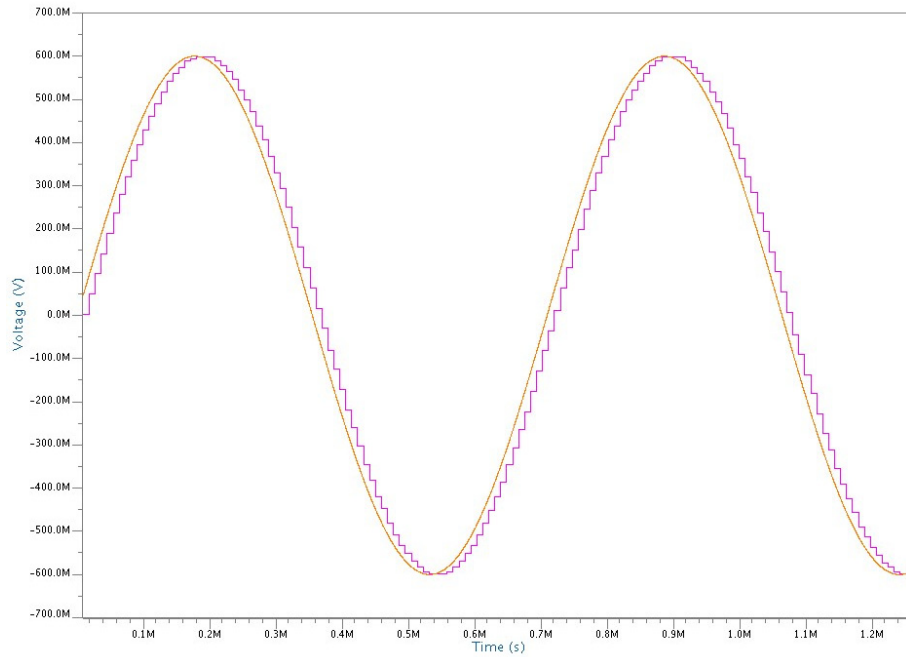


Figure 3.14: Transient response for an 8 bit ideal SA-ADC with a 1.4KHz full-scale sinusoidal and its corresponding digital output in decimal representation.

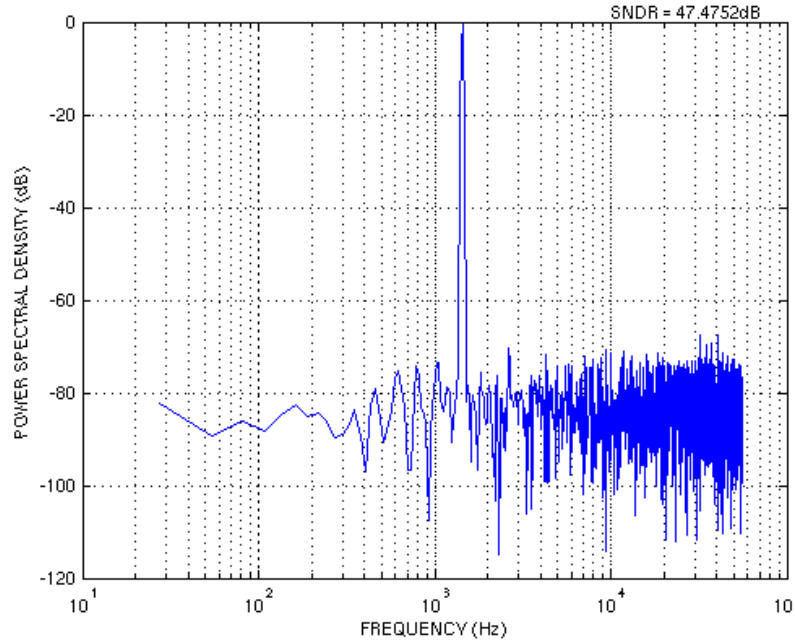


Figure 3.15: Output Spectrum FFT in 4096 points for an 8 bit ideal SA-ADC with a 1.4KHz full-scale sinusoidal

Transient analysis results for the 4 bit converter previously presented are shown in Fig. 3.12 with the digital output reconverted to its corresponding decimal values. The input signal is a rail-to-rail 1.2 V_{pp} with 0.6V common mode and 1.4KHz frequency. The FFT used 4096 points and Blackman Harris window. The corresponding output spectrum and SNR are shown in Fig. 3.13.

Fig. 3.14 shows the transient response of an 8 bit ideal SA-ADC for a 1.4KHz full-scale sinusoidal with digital codes represented in decimal values. The FFT used 4096 points and Blackman Harris window. The corresponding output spectrum and SNR are shown in Fig. 3.15.

Ideal performance is recorded for later comparisons through tracing the SNR with the normalized input amplitude in Fig. 3.16 then with the normalized input frequency (normalized to $f_s/2$) in Fig 3.17. The SNR-Ain curve is linear as predicted from Eq. 3.8. The maximum SNR equals the dynamic range at A_{FS} and the 0 dB SNR point is at $A_{in}/A_{FS} \approx -48\text{dB}$. The SNR is almost independant of the input frequency f_{in} .

From both curves, it is concluded that ideally the SA-ADC system allows rail-to-rail operation and an input Bandwidth equal to the Nyquist frequency without performance degradation. The components non-idealities presented in the next chapters will define the real maximum achievable performance with transistor level

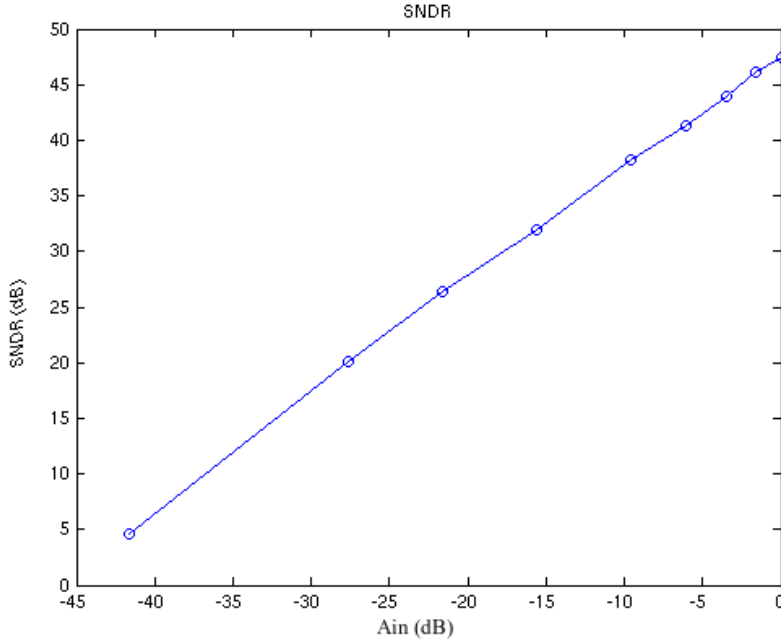


Figure 3.16: Signal to noise ratio SNR v.s. Normalized Input Amplitude A_{in} from 0 to V_{FS} for an ideal 8bit SA-ADC.

simulations.

An example of the generated control signals by the SAR algorithm for a double-reference DAC architecture is shown in Fig. 3.18. These are the reference switches gate signals controlled by the SAR for the case of a zero input signal. The result is a rotating '1' from the largest capacitor to the smallest one since the signal is at its minimum level.

Fig. 3.19 presents the digital clocks *clock1* and *clock2* and the control signals *start* and *invert* used in the VHDL testbench. Non overlapping clocks are needed to allow enough settling time for each block specially with transients sensitive block like the comparator. The generation of non-overlapping clocks on chip for the target frequencies is not problematic. It will rather add more freedom in selecting NMOS or PMOS input pairs for the comparator.

3.6 Conclusion

This Chapter presented the operation and possible system architectures of a successive approximation ADC. The dedicated sample-and-hold architecture is valid only in single-ended implementation and it is used for ultra-low-voltage and energy-limited applications. Double-reference charge redistribution and triple-reference ar-

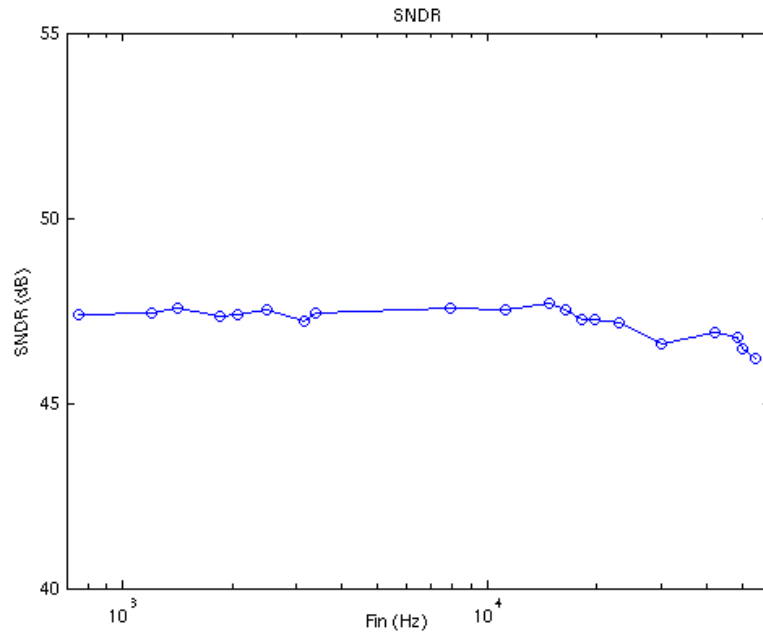


Figure 3.17: Maximum Signal to noise ratio SNR v.s. Normalized Input frequency f_{in} up to the signal Bandwidth for an ideal 8bit SA-ADC.

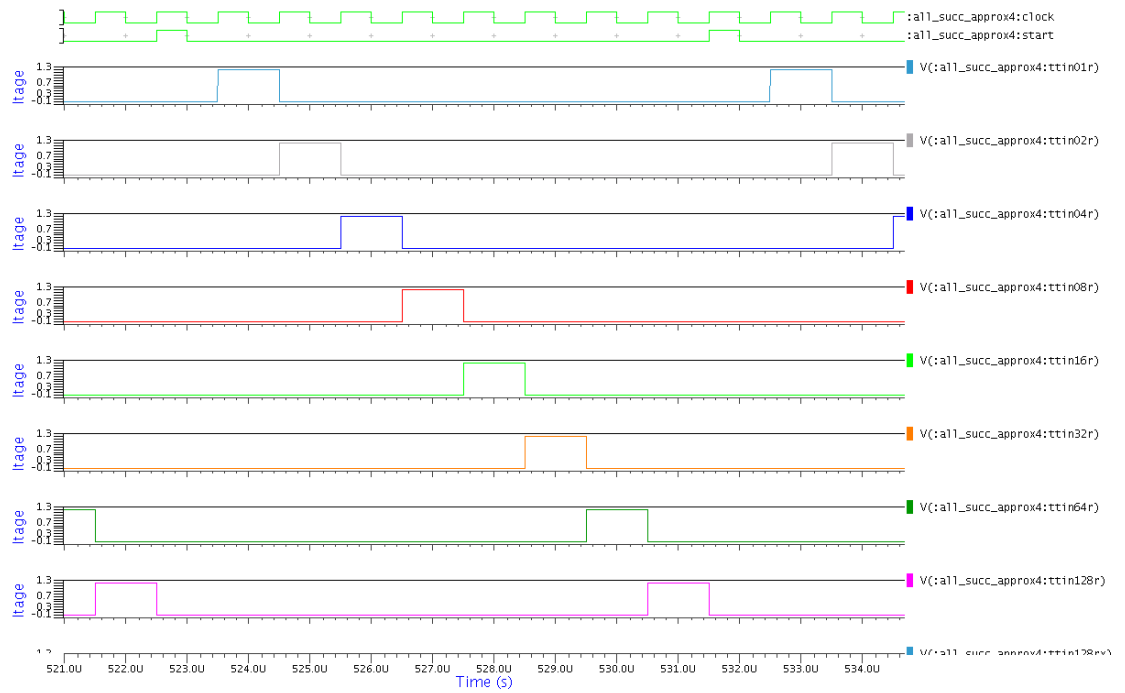


Figure 3.18: SAR control outputs for the reference switches during a search path with the '1' propagating from a switch to another

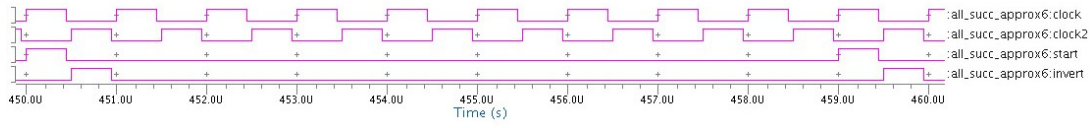


Figure 3.19: VHDL clocks and SAR control for the 8 bit SA-ADC

chitectures are used in wide bandwidth systems. These architectures are valid for both single-ended and differential implementations. A general VHDL-AMS SA-ADC model is written and a set of Eldo transient simulations were made. MATLAB is used for postprocessing the simulation results to characterize the system performance. Simulation results of 4, 6 and 8 bit ideal SA-ADCs were presented and compared with theoretical values. A small difference resides between the calculated and simulated values due to the selection of a moderate number of points (4096) in order to have resonable simulation time.

Successive Approximation ADC Circuit Design

4.1 Introduction

In this Chapter, different DAC architectures are presented in section 4.2. Thermal noise and capacitor non-idealities are presented in sections 4.3 and 4.4. The switches selection and sizing is discussed in section 4.5 and special switches are presented to solve the leakage problem in single-ended double-reference architectures, then the comparator circuit is analyzed in details in section 4.6. SAR algorithm implementation with digital gates is shown in section 4.7 and finally the non-overlapped clock generator circuit is in section 4.8.

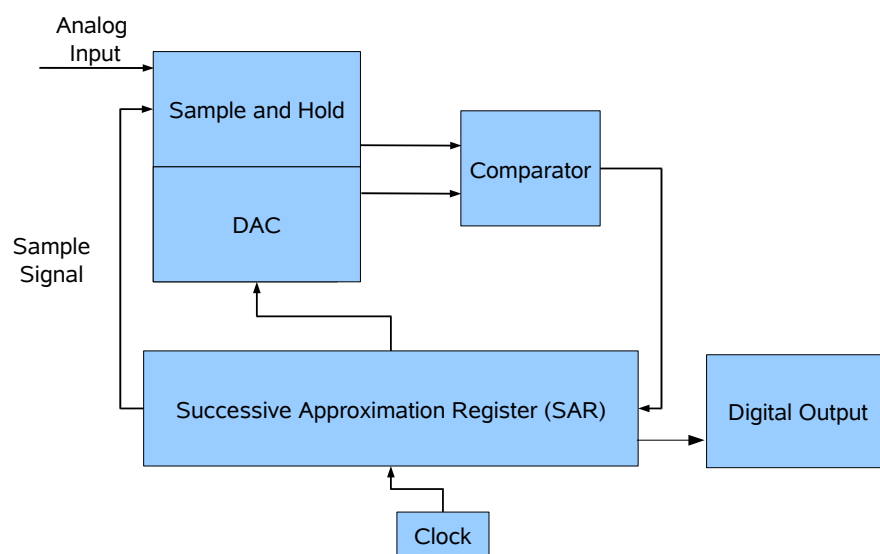


Figure 4.1: Successive approximation ADC system block diagram

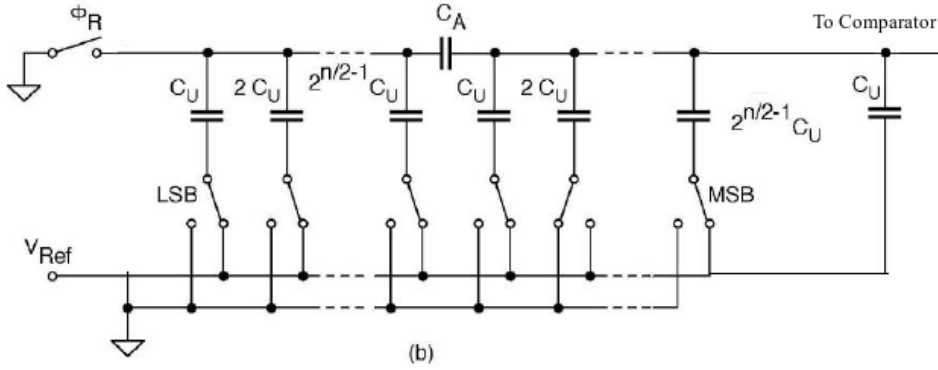


Figure 4.2: DAC with attenuation capacitance to reduce the capacitor spread.

4.2 DAC Architecture

Different DAC architectures were reported for use with SA-ADC depending on the application requirements: very low voltage at low frequencies [1]-[9], very low voltage and moderate bandwidth [29], low power and wide bandwidth [15]-[16]-[17]-[30]. For system demanding wide bandwidth or high resolution, the conventional binary-weighted capacitive DAC introduced in section 3.3 is no more suitable. Even with a unit capacitance as low as a 10 fF, the total capacitance will be about 3 pF because of the exponential dependence between the total capacitance and the resolution. Such value needs very high switch conductances for linear sampling and places stringent constraints on matching between unit capacitances.

4.2.1 Attenuator Method

Another DAC configuration [13]-[32] is shown in Fig. 4.2 where an attenuation capacitor C_A is used in the middle of the array to divide it in 2 parts limiting the maximum element in each to $2^{(n/2-1)}$. The MSB section is the right-hand part and the LSB section is at the left of C_A and the total capacitance is reduced and the capacitances count also is reduced to $2 \cdot 2^{n/2} - 1$.

The series of attenuation capacitance and the entire right array must equal C_u

$$C_u = \frac{C_A \cdot 2^{n/2} C_u}{C_A + 2^{n/2} C_u} \quad (4.1)$$

The disadvantages of this architecture are:

- Parasitic capacitance of the top plate of the left section may significantly affect the DAC output levels specially with C_A participating adding both its bottom plate and top plate parasitics.

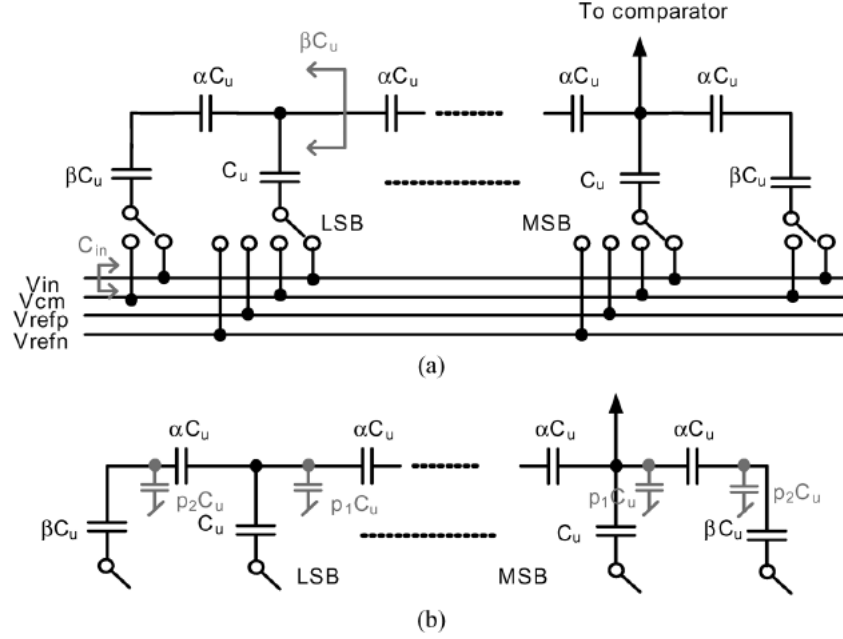


Figure 4.3: Series capacitive DAC with arbitrary radix (a) Ideal case without parasitic capacitance (b) inclusion of parasitic capacitance

- The Layout of C_A requires special care since it is a fraction of C_u

4.2.2 Reconfigurable Radix Method

Another approach for a DAC architecture with reconfigurable radix was reported to allow up to 4 GHz sampling frequency [16].

Shown in Fig. 4.3 (a), the DAC uses only three different sizes of capacitors ratios from $1:\alpha:\beta$ are used to build the ladder. The equivalent capacitance at every internal node is always $\beta \cdot C_u$. Therefore, the charge redistribution from one section to the adjacent one always sees the capacitive divider between $\alpha \cdot C_u$ and $\beta \cdot C_u$. The selection of this division ratio will change the DAC radix. In consequence, the radix of the SAR algorithm is also reconfigurable.

According to this, the design equations for the DAC in the ideal case are then:

$$\begin{aligned} \beta &= 1 + \alpha \parallel \beta \\ Radix &= 1 + (\beta/\alpha) \end{aligned} \quad (4.2)$$

Due to the series connection of the capacitors, the equivalent capacitance decreased, which reduces the DAC settling time and the total input capacitance. This will relax the requirements needed in matching and layout.

The traditional trade-off between matching property and total input capacitance

is removed since it does not depend on reducing the unit capacitance size. The total input capacitance of this DAC is no longer dependent on the number of ADC bits and is calculated as

$$C_{in} = [1 + 2 \cdot (\alpha \parallel \beta)] \cdot C_u \quad (4.3)$$

If the values of α and β are both chosen to be 2, then substituting in Eq. 4.2 will result in a radix = 2 (binary radix) and an input capacitance of only $3C_u$. In this case all vertical capacitors equal $2C$ and all horizontal capacitor equal C except those on both extremities equal $2C$. This configuration is called a C-2C DAC.

Like the attenuator method, the potential issue with this structure is the vulnerability to the parasitic capacitance as shown in Fig. 4.3 (b) due to the capacitor parasitics which will affect the radix and the error will spread exponentially. The following change in the design equations is needed to account for parasitic estimation.

$$\begin{aligned} \beta &= 1 + \alpha \parallel \beta' + p_1 \\ Radix &= 1 + (\beta'/\alpha) \\ \beta' &= \beta + p_1 \end{aligned} \quad (4.4)$$

Solving Eq. 4.2 and Eq. 4.4 we get the new ratios (α_{mod} and β_{mod}) relations with the original ones (α_{org} and β_{org}):

$$\begin{aligned} \alpha_{mod} &= (1 + p_1) \cdot \alpha_{org} \\ \beta_{mod} &= (1 + p_1)\beta_{org} - p_2 \end{aligned} \quad (4.5)$$

Finally, this configuration will be also very sensitive to routing parasitics and layout will need caution and common centroid symmetry.

4.3 Thermal noise

The thermal noise results from sampling a signal and depends on the value of the sampling capacitance. In charge redistribution architectures the sampling network is made by the switch resistance and the total DAC capacitance.

The thermal noise is also called the kT/C noise, where k is the Boltzman constant, T is the temperature and C is the sampling capacitance. It will place a first limitation on the minimum value of the total DAC capacitance, thus on the unit capacitance C_u . For moderate resolutions of 6-8 bits SA-ADC it was proved [1]-[16] that the ADC is not limited by the kT/C noise even with unit capacitance values as low as 10 fF.

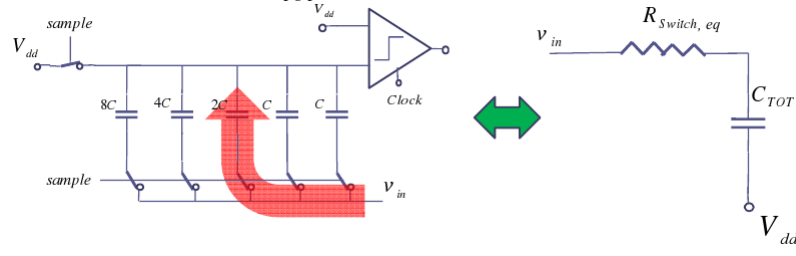
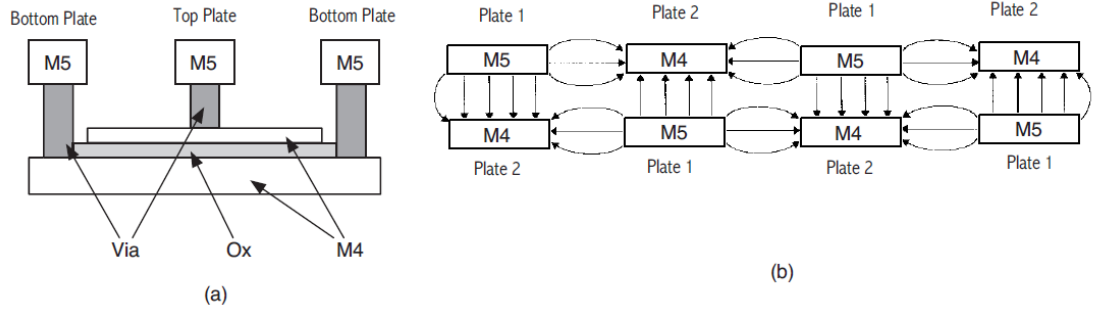
Figure 4.4: kT/C noise affecting a sampling network

Figure 4.5: (a) MIM capacitance (b) MMCC capacitance

4.4 Capacitors Non-Idealities

Integrated capacitances are made from two conductive plates separated by a thin layer of oxide and located a few microns or less from the substrate. There are two main configurations: with plates one on the top of the other (the capacitor can be poly-oxide-poly or Metal-Insulator-Metal, MIM, Fig. 4.5 (a) or with plates made of side by side fingers of metals (Metal-Metal Comb Capacitor, MMCC) as shown in Fig. 4.5 (b) [13].

4.4.1 Parasitics Effect

Since the structures are close to the substrate in both cases, the parasitic from the plates to the substrate is not negligible. The poly-poly and the MIM have a bottom plate that partially shields the top one thus giving a top plate parasitic that is smaller than that of the bottom plate. The two parasitic capacitances of the MMCC structures are almost equal. Also, for MIM and MMCC the use of high level metals is recommended for a small parasitic with the substrate.

The parasitic of the plate connected to V_{ref} or ground does not affect the capacitive divider as it receives the required charge by low impedance nodes. Instead, the

parasitic capacitances connected to the output node affect the capacitive division between output and ground. The output voltage for a binary-weighted array of capacitors becomes

$$V_{out} = V_{ref} \frac{\sum_1^n b_i C_i}{\sum_0^n C_i + \sum_0^n C_{p,i}} \quad (4.6)$$

where b_i are the bits of the digital control and C_i and $C_{p,i}$ are the nominal value and parasitic associated with the unity elements of the array. If the parasitic capacitances are independent of the output voltage, Eq. 4.6 leads to an attenuation the generated voltages at the comparator input by a factor of α but will not affect its sign which is the information relevant for determining the bit. However, non-linear parasitics that change with the output voltage cause harmonic distortion.

$$\alpha = \frac{C_u 2^n}{C_u 2^n + C_p} \quad (4.7)$$

This is an important advantage for conventional binary-weighted DAC, where parasitics of the upper plates will add up and their sum will contribute with the routing parasitics as an offset independent of the signal value. This offset may be easily removed in the digital domain. Those of the bottom plates are always connected to a reference voltage and will not affect the signal or the DAC levels. But this is not the case of other DAC configurations like the attenuator or the reconfigurable radix that suffer parasitics sensitivity. Their parasitics, having different values will also cause harmonic distortion.

4.4.2 Mismatch Effect

In the fabrication, many factors may lead to capacitor ratio errors, such as the undercutting of the mask which defines the capacitor. This problem can be circumvented by building large capacitors from parallel identical size unit capacitances. Thus ratios between capacitors are not affected by undercut. Other factors may contribute more mismatch such as shadowing, etching and in case of poly-oxide-poly capacitors, the oxide thickness gradients [23]-[27]-[33]. The main solution for enhancing the capacitors matching is through the use of common centroid layouts.

Mismatch in binary capacitor ratios will not give rise to offset or gain errors. For either zero or full-scale input, no net charge redistribution between capacitors occurs and all capacitors are either fully discharged or fully charged, respectively. Thus, a gain error is not possible because the end points of the transfer function curve, V_{out} vs. V_{in} , are not dependent on capacitor matching. For the same reason, no offset error can arise from capacitor mismatch since the mismatch cannot be manifested unless a charge redistribution exists in the final configuration.

On the other hand, mismatch in the binary ratios leads to harmonic distortion. The linearity is very sensitive to the fractional change in the large capacitors but not very dependant upon similar fractional changes in the smaller capacitors.

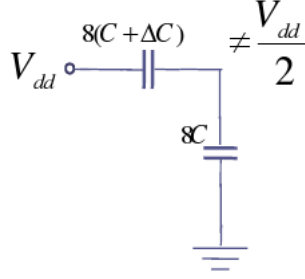


Figure 4.6: Mismatch effect

It should be pointed out that normally all capacitors have simultaneous deviations which cause ratio errors and the worst case combination of these must always be considered. The optimization of the ratio accuracy in the array is a prime consideration.

Capacitor mismatch $\Delta C/C$ will add a second limitation on the minimum value of C_u and for N bits binary-weighted array [29]

$$\sigma_{DNL}^2 = \frac{2^N - 1}{2\sigma^2(\Delta C/C)} \quad (4.8)$$

4.4.3 MIM Capacitors

A MIM capacitor is made of high density metals in order to use smaller areas. It presents a good linearity since its value doesn't change with voltage across its terminals or with temperature.

Modern technologies offer dedicated metal layers for drawing MIM capacitors. Similar to the poly-poly capacitor, the MIM bottom plate is larger than its top plate

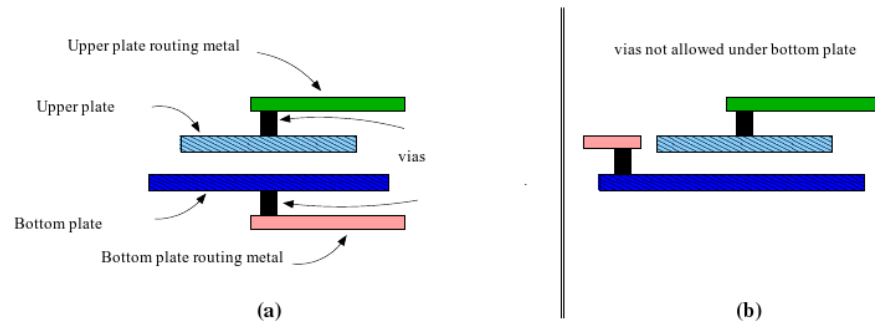


Figure 4.7: MIM capacitor cross section (a) Routing via under the bottom plate. (b) Routing via above the bottom plate

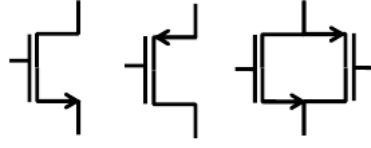


Figure 4.8: Common switches

which ensures the superposition of the plates even with fabrication deviations which may change their relative positions.

There are 2 possible common ways to realize a MIM capacitor described in Fig. 4.7. The one shown in (a) makes a via under the bottom plate to connect it to the routing metal different than the one used for the upper plate routing. But the second form (b) can use a single metal for routing both upper and bottom plates. Some technologies prevent the use of the configuration (a) like the one used in this thesis ST 0.13

The precision error of the MIM capacitors is dominated by the etching errors and it contributes a relative error

$$\frac{\Delta C}{C} \approx \frac{-2\Delta_E P}{A} \quad (4.9)$$

where C is the capacitance nominal value, ΔC is the change in the capacitance value, Δ_E is the etching error, P and A are respectively the perimeter and the area of the top plate. So it is the error is proportional to the ratio P/A that's why we try to draw a MIM capacitor as a square, the form that minimize the ratio P/A for a given capacitance value [34].

4.5 Switches

The selection of switches is according to the signal range needed to be switched, usually NMOS switches are used to connect to ground, PMOS switches are used to connect to V_{dd} and CMOS switches are used to switch intermediate voltages between ground and V_{dd} . Special low-voltage switches are implemented for the case where $V_{tn} + V_{tp} > V_{dd}$ because of the degradation of the switch conductivity. Lowering the transistor threshold voltage by ion implantation for example raises the cost of fabrication, while clock boosting has reliability issues like oxide breakdown and drain induced barrier lowering DIBL [35].

The problem that emerged in the operation of the single-ended ADC presented in section 3.3.2 needs a special switch to handle. A charge pump switch was proposed in [1] but another bootstrap configuration first implemented in [28] for switching

rail-to-rail low voltage signals may also be modified to solve this problem.

The parasitics of the switches in the SA-ADC won't affect the accuracy of the conversion because these parasitics are always either discharged to ground or charged to V_{ref} but never absorbs charge from the top plate. Therefore for low and moderate frequencies, the switch devices can be quite large permitting rapid redistributions.

4.5.1 Switch Resistance

The switches ON resistance is a limiting factor of the possible conversion rate as a MOS transistor in the linear mode will have a resistance of:

$$R_{ON} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_t)} \quad (4.10)$$

Then for charging N capacitors, N switches are connected to the capacitor bottom plates while only one switch is connected to the top plates

$$R_{ON,eq} = \left[\frac{1}{N \mu_{bot} C_{ox} \frac{W_{bot}}{L_{bot}} (V_{GS,bot} - V_{t,bot})} + \frac{1}{\mu_{top} C_{ox} \frac{W_{top}}{L_{top}} (V_{GS,top} - V_{t,top})} \right] \quad (4.11)$$

$$\tau = R_{ON,eq} C_{total} \approx C_{total} \frac{1}{\mu_{top} C_{ox} \frac{W_{top}}{L_{top}} (V_{GS,top} - V_{t,top})} \quad (4.12)$$

Though the sampling rate is $f_{clk}/(N+1)$ but actually the sampling duration is only $t_{clk}/2$, so the DAC settling time and the latched comparator decision time will impose limitations on the maximum value of sampling time constant. Sampling can be made on many clock cycles but the comparator has to take decisions within half the clock period to allow the reset phase. A value of 3τ is found as the time necessary for the DAC output to settle to 98% of the final value so If the minimum unit capacitance is chosen and the sampling time constant is not adequate for linear sampling, an increase in the switches sizes will help decreasing the sampling time constant. Another method is to allow sampling over more clock cycles [30]

$$\frac{t_{clk}}{2} > 3\tau, \quad \tau = R_{ON,eq} C_{total} \quad (4.13)$$

The maximum sampling frequency is limited by the time constant of the equivalent resistances of all switches with the total capacitance of the array.

4.5.2 Charge Injection

The channel charge of a MOS transistor is the total charge in the inversion layer and is expressed as

$$Q_{ch} = W L C_{ox} (V_{dd} - V_{in} - V_{th}) \quad (4.14)$$

When the switch turns off, Q_{ch} exits through the source and drain terminals.

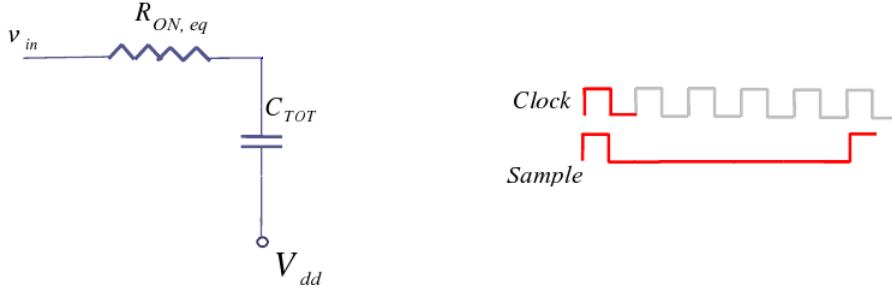


Figure 4.9: Equivalent circuit during sampling considering MOS switch resistance

In Fig. 4.10 (a) the charge injected to the left side is absorbed by the source with no error but the charge injected to the right side is deposited on C_H , introducing an error in the voltage stored on the capacitor. The fraction of charge that exits through the source and drain terminals is a complex function of various parameters such as the impedance seen at each terminal to the ground and the transition time of the clock. Furthermore, in many cases, these parameters are poorly controlled and most circuit simulation programs model charge injection quite inaccurately. As a worst case estimate, we can assume that the entire channel charge is injected onto the sampling capacitor such that

$$V_{out} \approx V_{in} - \frac{WLC_{ox}(V_{dd} - V_{in} - V_{th})}{C_H} \quad (4.15)$$

The usual solution for charge injection problem is the use of a dummy switch with a complementary clock to the original switch as shown in Fig. 4.10 (b) in such a way that the charge absorbed by this dummy switch when it activates δq_2 almost eliminates the charge injected δq_1 , the use of CMOS switches and differential structures also helps eliminating this problem.

Charge injection is not a major problem for the SA-ADC because most of the nodes are actively driven during all phases of the conversion cycle. The only charge injection event during the conversion cycle is the opening of the reference switch at the end of the input sampling period. The resulting error voltage is very small as the charge is injected onto the entire array. Moreover the error is systematic because the reference switch always has the same terminal voltages, resulting in an overall offset to the ADC which is always less than 0.1 LSB. [36]

4.5.3 Charge-pump Switch

The charge-pump switch[1] and its associated waveforms are presented in Fig. 4.11. By boosting the gate (and body) of the switch to approximately $1.5V_{ref}$ during the off state, the circuit guarantees that the switch will remain strongly off when the drain voltage equals $1.5V_{ref}$. When CLK is low, the switch is on and V_{comp} is forced

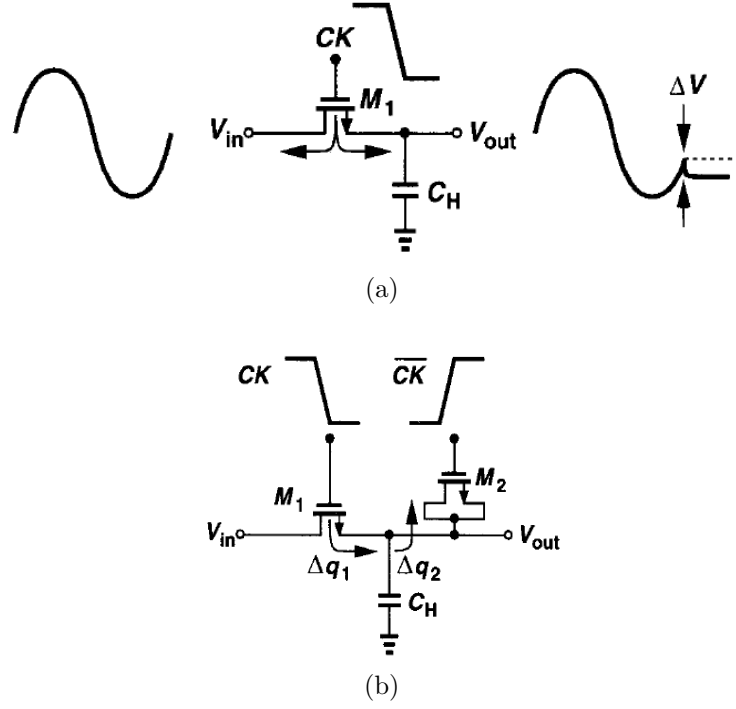


Figure 4.10: (a) Charge injection effect (b) Charge injection cancellation with dummy switch

to V_{ref} through M_1 , Device M_4 is off, and M_2 charges the body of M_1 and drain of M_4 to $V_{ref} - V_{tn2}$. When CLK goes high, the switch transitions to the off state. Device M_3 is off, M_4 is on, and the gate and body of the PMOS switch M_1 are overdriven to $2V_{ref} - V_{tn2}$, by the charge previously pumped into C_{hold} .

This circuit does not eliminate charge leakage for arbitrary search algorithms mentioned in section 3.4. The maximum voltage at the DAC output for such algorithms is $2V_{ref}$ yielding a worst case off state for M_1 equals V_{tn2} which has a value very near to V_{tp1} . Another drawback is that during the operation the reverse source-gate voltage may exceed the supply voltage if the *comp* terminal has a zero voltage while the gate is pre-charged to $V_{ref} - V_{tn2}$. This drawback can be eliminated by the bootstrap switch on the expense of more circuit complexity.

4.5.4 Bootstrap Switch

The basic idea of the bootstrap switch[28] is presented in Fig. 4.12.

The signal switch is transistor M_{NSW} while the five additional switches S_1 - S_5 and the capacitor C_{offset} constitute the bootstrap circuit. During ϕ_2 , switches S_3 and S_4 pre-charge the capacitor to V_{dd} while switch S_5 fixes the gate to V_{ss} to ensure

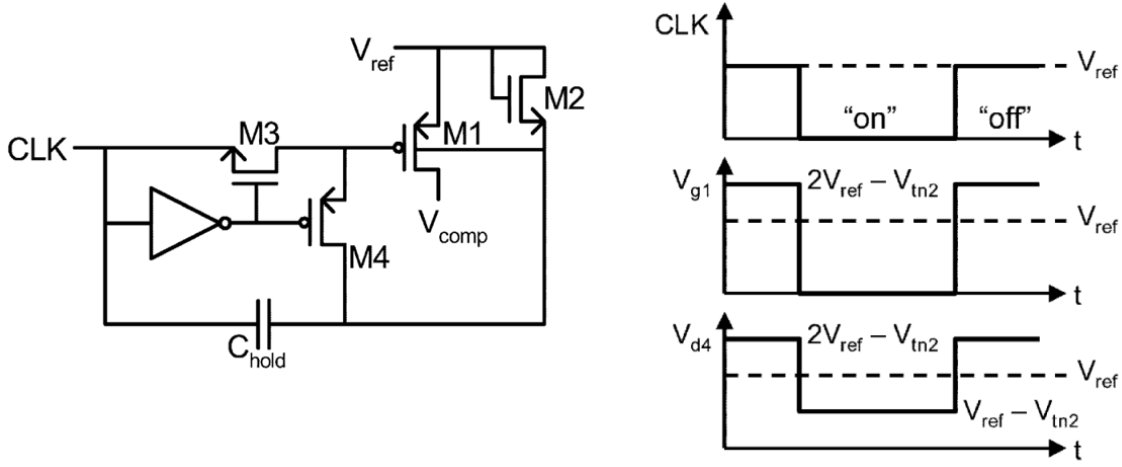


Figure 4.11: Charge-pump switch circuit with associated waveforms

the main switch MNSW is turned-off. During ϕ_1 switches S1 and S2 connect the pre-charged capacitor between the gate and source of MNSW such that the gate source voltage V_{GS} is equal to the voltage V_{dd} across the capacitor. MNSW will have a gate source voltage independent of the switched voltage and will keep good linearity to switch V_{dd} to the DAC upper plates.

While MNSW is turned-off with V_{SS} , the DAC voltage is varying from V_{ss} to $2V_{dd}$ as a worst case for arbitrary search algorithms and the leakage problem is resolved. To preserve reliability another series modified bootstrap switch is recommended. Where the first is connected to V_{dd} and its gate is tied to V_{ss} in the off-state while the gate of the second bootstrap connected to the DAC is tied to V_{dd} to shield the former.

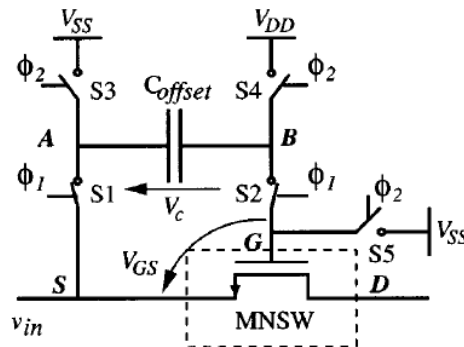


Figure 4.12: Basic switch bootstrapping circuit

4.5.5 Bootstrap Switch Circuit

This section describes the circuit implementation of the bootstrapped switch shown in Fig. 4.12. The transistor level circuit of the bootstrapped switch is illustrated in Fig. 4.13. Transistors MN1, MP2, MN3, MP4 and MN5 correspond to the ve ideal switches S1-S5 respectively. Additional transistors and modified connectivity shown in Fig. 4.13 were introduced to extend all switch operation from rail-to-rail while limiting all gate-source voltages to V_{DD} . It is evident that the worst case input signal (with respect to switch operation) is that of $V_{in} = V_{DD}$, which is the value attributed to v_{in} in the discussion hereafter.

MN1 has to switch V_{dd} to make the circuit fully efficient. For this reason, its gate voltage is also bootstrapped, i.e. connected to the gate of MNSW. Additional critical problems arise on nodes B and G as their voltages reach $2V_{dd}$ due to bootstrapping: First of all, transistor MP4 must remain OFF during ϕ_1 in order not to loose the charge stored on C_{offset} during ϕ_2 . If the clock is used to drive it as shown in Fig. 4.12, its gate-source voltage would be $-V_{dd}$ and the transistor cant be turned-off. Thats why its gate is connected to node G which provides a voltage of $2V_{dd}$ during ϕ_1 cutting-off the transistor, and a voltage of V_{ss} during ϕ_2 which ensures its high conductivity.

Secondly, the gate-source voltage of transistor MP2 could reach $2V_{dd}$ during ϕ_1 causing reliability problems. In Fig. 4.13 a solution is proposed. Transistor MN6 is used to connect the gate of MP2 (node E) to node A thus keeping its gate-source voltage equal to $-V_{dd}$ (the voltage across C_{offset}) during ϕ_1 . During ϕ_2 transistor

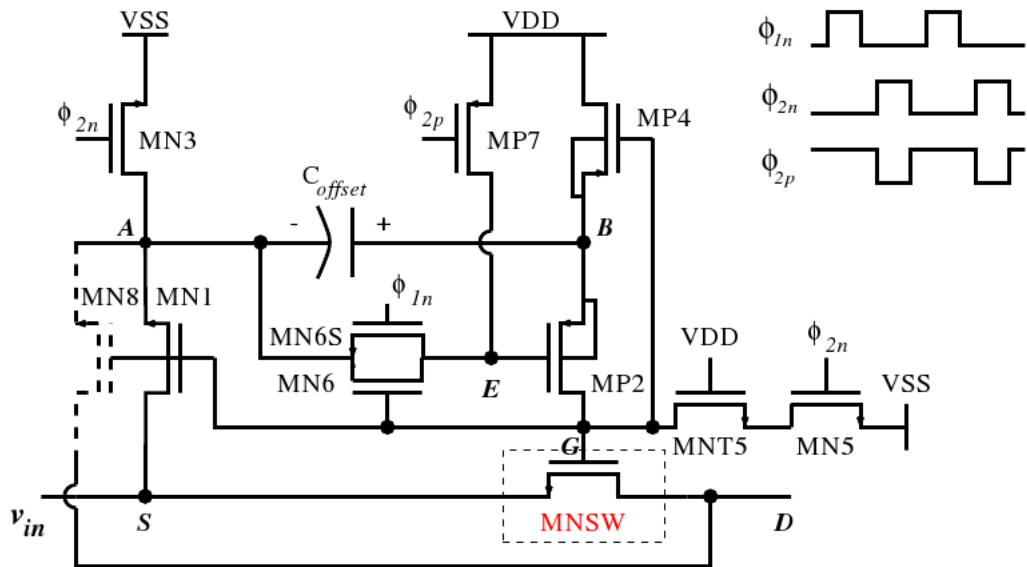


Figure 4.13: Circuit implementation of the bootstrap special switch

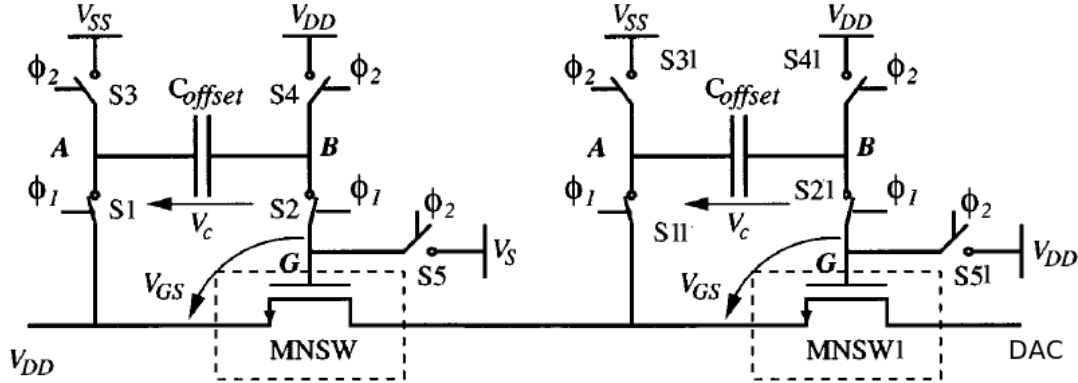


Figure 4.14: Basic switch bootstrapping circuit with shielding modified bootstrap

MP7 connects it to VDD turning it off.

The gate of MN6 is tied to node G to keep it conducting as the voltage on node A rises to V_{dd} during ϕ_1 . There is thus a dependency loop inhere; In order to turn on MN6, it must have a sufficient gate-source voltage i.e. MP2 must then be conducting! Transistor MN6S is then necessary as a startup to force transistor MP2 to conduct. when ϕ_1 goes high, transistor MN6S is turned on since its source (node A) is discharged to V_{ss} at the beginning of ϕ_1 . Node E thus goes from V_{dd} to V_{ss} through transistor MN6S, this turns on transistor MP2 and consequently the voltage on node G begins to rise turning on transistors MN1, MN6 and MNSW. Node A is, hence, connected to the input and point G rises to $V_{dd} + v_{in}$.

It should be also noted that for an NWELL process, the bulk of transistors MP2 and MP4 must be tied to the highest potential i.e. node B, and not to V_{dd} in order to prevent latch-up. Lastly, transistor MNT5 has been added in series with MN5 in order to prevent the gate-drain voltage of the latter from reaching $2V_{dd}$ during ϕ_1 . The bulk of MNT5 is, however, tied to V_{ss} . During ϕ_1 when it is off, its drain-bulk diode junction voltage reaches a reverse bias voltage of $2V_{dd}$. Typically a CMOS technology is designed such that the reverse breakdown of a stand-alone n+/p- junction is approximately $3V_{dd}$ [35].

MN8 is added for fully symmetry of the bootstrap switch. If the lower voltage terminal can not be determined at the start of conduction, switch symmetry is needed to avoid oxide overstress during transients. This is not needed in the single-ended double-reference SAR-ADC, where the sampling operation always starts with the final DAC voltage reset to V_{dd} .

Since the bootstrap switch is designed to prevent any gate-source voltage more than V_{dd} . The use of one bootstrap switch will solve the leakage problem even with

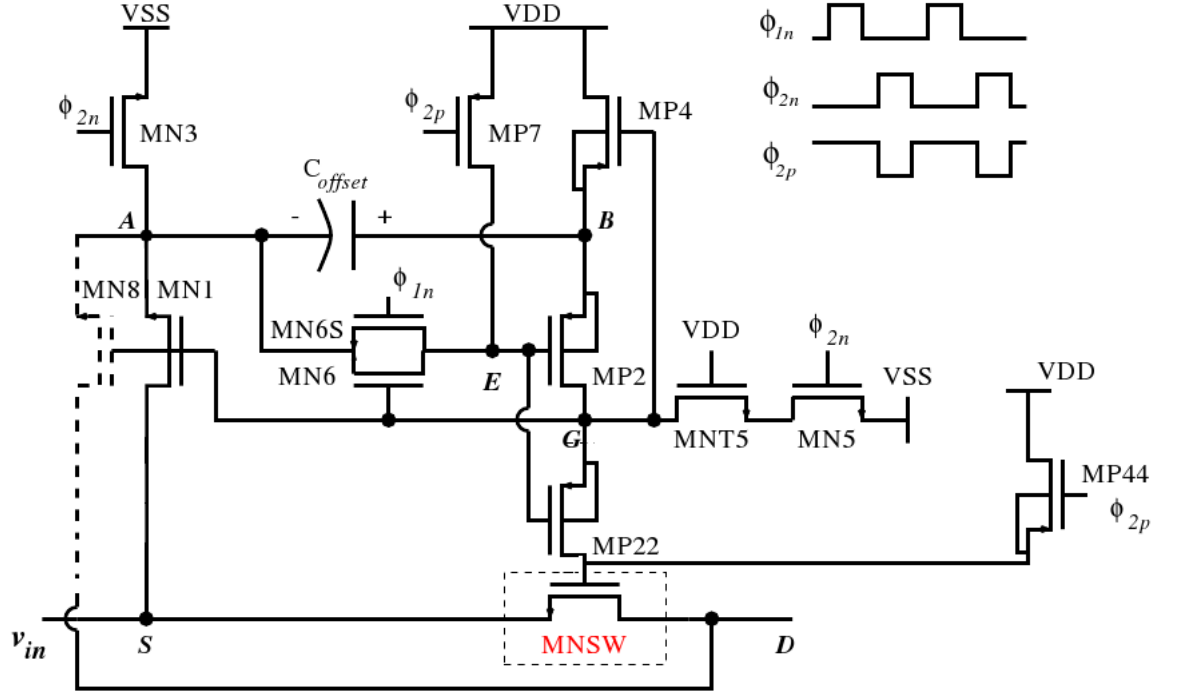


Figure 4.15: Circuit modification of the bootstrap special switch

arbitrary searches where the DAC voltage worst case is $2V_{dd}$. But since the DAC voltage vary from V_{ss} to $2V_{dd}$ this will cause reliability problem when the switch is turned-off by V_{ss} . A modified bootstrap in Fig. 4.14 was added in series with the original, during the turn-off phase, its gate will be tied to V_{dd} shielding the intermediate node from the possible $2V_{dd}$ value on the DAC.

At the circuit implementation, 2 additional transistors were added, MP22 is symmetrical with MP2, it connects the node G to the gate of the main switch MNSW during ϕ_1 to maintain the normal bootstrapped operation, then it disconnects the whole upper circuit from the gate of MNSW during ϕ_{2p} , the off-state of the main bootstrap switch. MP44 ties the gate of MNSW to V_{dd} during ϕ_{2p} shielding the main bootstrap switch from DAC voltages higher than V_{dd} .

4.6 Comparator

The comparator is the only active block in the SA-ADC and its specifications may affect the ADC resolution. Fig. 4.16 illustrates how an error of comparison in identifying the fourth bit propagates along all the successive steps. It leads to another search path and thus an error of 2LSB which will translate into a static code error and an increase in the harmonic distortion. The key parameters of the comparator

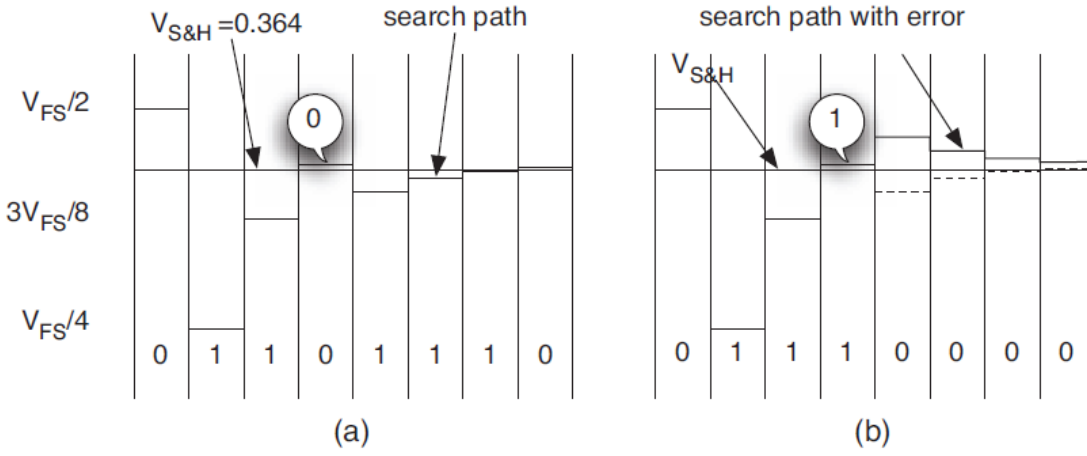


Figure 4.16: (a) Correct search path (b) Search path with error at the fourth clock period

performance are discussed in this section:

4.6.1 Meta-stability

The meta-stability error occurs when the output of a comparator is undefined. Typically a sampled-data comparator is realized using a pre-amplifier and a latch. During one phase the input signal is pre-amplified and during the latch phase a regenerative circuit fixes the logic level. If the input differential voltage $V_{in,d}$, is not large enough the comparator output may be undefined at the end of the latch phase giving an error in the output code. The differential latch of Fig.4.17 is the positive loop of two transconductors whose regenerative time constant, τ_L , depends on the parasitic capacitance C_p at the output node and the transconductance g_m of the regenerative latch.

$$\tau_L \approx \frac{C_p}{g_m} \quad (4.16)$$

The meta-stability error probability can be approximated by

$$P_E = \frac{V_0}{V_{in}A_0} e^{\frac{-t_r}{\tau_L}} \quad (4.17)$$

Where V_0 is the voltage swing required for valid logic levels and t_r is the period of the latch phase and A_0 is the pre-amplifier gain. f_{ck} is the clock frequency and normally the latch phase equals $1/2f_{ck}$. The comparator has to ensure an almost certain output for V_{in} larger than $V_{LSB}/2$ with a probability $P_{E,max}$. This probability

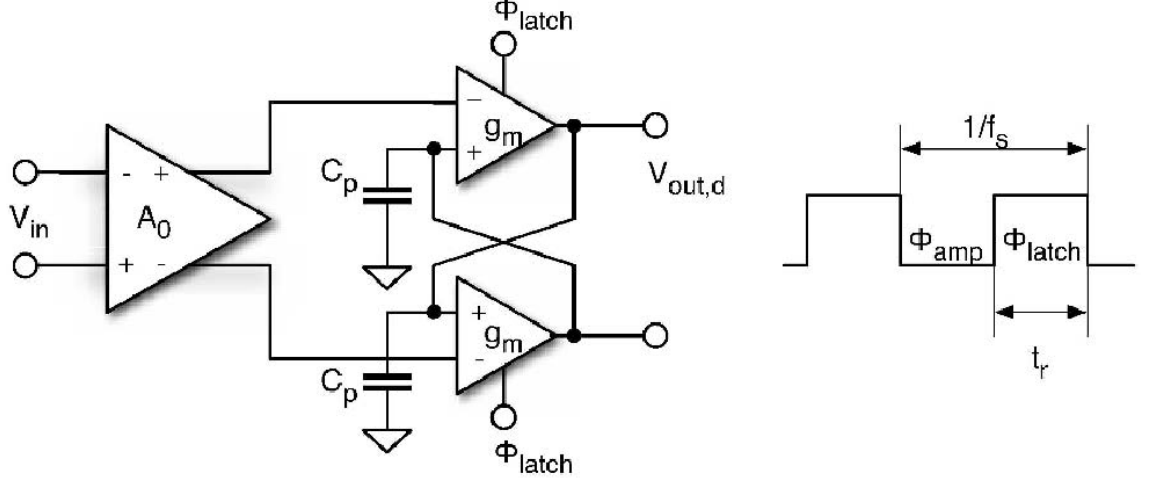


Figure 4.17: Typical comparator used in data converters

has to have the following boundary:

$$f_{ck} \cdot \ln \left[\frac{V_0 2^{n+1}}{P_{E,max} V_{FS} A_0} \right] < \frac{1}{2\tau_L} \quad (4.18)$$

For more resolution and speed, large g_m/C_p ratios are needed

4.6.2 Offset

Since comparator offset is added to the differential input it modifies threshold transition, it is needed for the comparator offset not to exceed $V_{LSB}/2$ for not affecting output. Though this offset error can be removed either in the analog or digital domain since it is signal in dependant, special care is to be paid for the design and layout of the pre-amplifier for a minimum threshold, transconductance parameter μC_{ox} and aspect ratio (W/L) mismatches in the input differential pair and active loads. The variation in the threshold voltage in this case could be estimated by

$$\Delta V_{th} = \frac{A_{VT}}{\sqrt{WL}} \quad (4.19)$$

Where A_{VT} is a technology parameter, and in case that the length of the MOS transistors are close to their minimum then the μC_{ox} and the $\Delta W/W$ mismatches are negligible and much lower than the relative length mismatch $\Delta L/L$, the MOS comparator offset is described from [13] by

$$V_{os,MOS} = \sqrt{\frac{A_{VT}^2}{WL} + \left[\frac{V_{GS} - V_{th}}{2} \right]^2 \frac{\Delta L^2}{L^2}} \quad (4.20)$$

4.6.3 Other Performance Parameters

The following parameter definitions are to be considered in the comparator design:

Resolution: The comparator resolution is the minimum voltage V_{res} that can be detected at the input and handled correctly which in the SA-ADC has to be at least $V_{LSB}/2$. With a low-voltage supply, settling time increases

Settling Time: The time needed by the comparator output to reach the steady state value of the right decision

$$T_{settling} = \frac{\tau_L}{A_0 - 1} \cdot \ln \frac{V_{FS}}{V_{res}} \quad (4.21)$$

Hysteresis: This is a dynamic performance parameter measuring an eventual phenomenon of memorizing. Usually, it results from an incomplete discharge of the internal nodes between 2 comparisons, which will imply a decision taking affected by the previous operation.

Kickback Noise: Since the comparator is a non linear device with internal nodes susceptible to present large voltage variations, typically of magnitude near the reference supply voltage which could be then coupled to the comparator input terminals across the drain-gate parasitics of the input transistors. This coupling give rise of kickback noise which could affect severely the circuit preceding the comparator specially if it has a weak output impedance.

4.6.4 Comparator Circuit

The comparator of Fig. 4.18 represents a classic latched comparator [10] controlled by the drains. We can analyze it as 4 connected blocks:

- Bistable block: MP11, MN7 and MN8, MP12
- Pre-charge block: MP15 and MP16
- Switching block: MN5 and MN6
- Input block: MN1 and MN2

At the pre-charge phase (clock low) the comparator outputs Q_p and Q_n (inputs of the bistable) are initialized to V_{dd} . At the comparison phase (clock high), the voltage difference between V_e and V_{ref} is transferred, injected as current at the nodes X and Y of the bistable which will then regenerate the outputs to V_{dd} and V_{ss} . The pair of switching transistors prevent the current flow in the branches during the low level of the clock. The circuit is classified as semi-dynamic since it does consume current only during the clock pulse and the difference with fully dynamic is that the latter is usually suitable for non-asynchronous configurations because its automatically reset once the output decision is ready.

The operation of the comparator can be then summarized in 3 phases:

- Static gain by the input pair to turn on the latch during time T_{init}
- Dynamic gain till the latch feedback gain becomes positive at instant T_z
- Latching the outputs T_{latch}

In the first phase, transistors MN1 and MN2 offer gain during T_{init} to charge the capacitances at nodes X and Y until the CMOS latch (bistable), MN7,MP11, MN8, MP12 turns on, this period is given by

$$T_{init} \approx \frac{C_{init} V_{th,M1}}{I_{ds,M1}} \quad (4.22)$$

The second phase starts when the latch turns on but the loop gain is still insufficient for positive feedback, this period is characterized by a dynamic time varying gain till instant T_z , this dynamic gain is

$$G_{dyn} = (T_z - T_{init}) \frac{g_{m,A}}{C_p} \quad (4.23)$$

When the latch gain is enough for positive feedback $G_{dyn} > 1$ at T_z the regeneration phase starts and its period is expressed by

$$T_{latch} = \frac{\tau_L}{A_0 - 1} \cdot \ln \frac{V_{FS}}{V_{res}} \quad (4.24)$$

The sum of the three phases durations defines the comparator decision time.

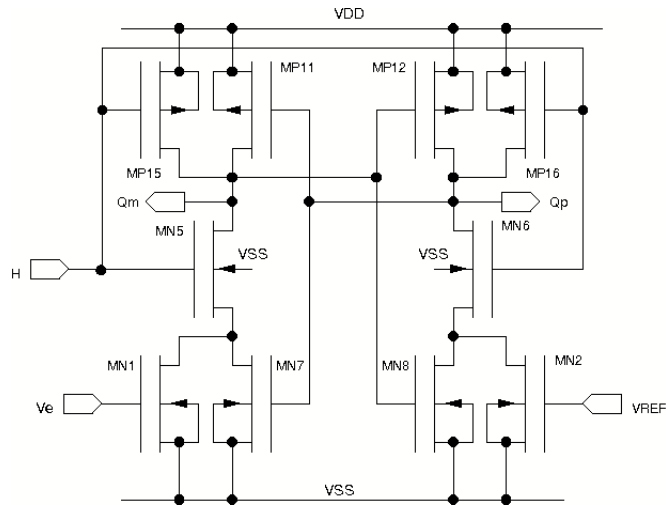


Figure 4.18: Semi dynamic generic comparator switched at the drains

4.6.5 Circuit Synthesis Parameters

A comparator is a non linear block and so the constituting MOS transistors have different operating points changing dynamically. Unlike the linear devices, it is impossible to consider for each transistor a rest point allowing an analytic determination of the dynamic primary parameters (g_m , g_{ds} , ...) to study the performance parameters (static gain, transition frequency,.....). We can only consider some general principles allowing sizing of the devices although the obtained performance parameters have to be confirmed with electrical simulations.

The switching and pre-charge pairs can be chosen as minimum size switches to minimize their parasitics contribution in the comparator settling time. The sizes of the bistable pairs and the input pair can not be selected in a similar straightforward way, many trade-offs exist and iterations are needed to find suitable values.

The duration of dynamic gain is difficult to analyse, besides its almost negligible with respect to T_{init} and T_{latch} . So it may be neglected without affecting much the design. The bistable transistors sizes will be chosen to realize a fast settling time and load capacitance independence. Substituting for the assumed linear gain in Eq. 4.21 it becomes

$$T_{settling} \approx \frac{C_{Qp} \cdot r_o/4}{g_m/(r_o/4)} \cdot \ln \frac{V_{FS}}{V_{res}} \quad (4.25)$$

Since r_o decreases when W/L increases and g_m increases with W/L, in Eq. 4.25, a fast settling time can be achieved by increasing W/L. According to [37] this increase is limited by

- The minimum area allowed to keep the offset voltage in Eq. 4.20 as low as possible
- the corresponding increment in the parasitic capacitance.

For a latch time independent of the load capacitance, the width should be increased while the length has to decrease [10]. The input pair sizes are chosen to minimize T_{init} . This pair is assumed in saturation since a linear gain is needed for the differential input to be amplified and applied to the latch input. Also, with the input pair in saturation the comparator offset decreases. From Eq. 4.22 high current is demanded to decrease T_{init} but the parasitic capacitance, C_{init} charged before the latch turns on demands reduced transistor area. Both demands may be achieved by decreasing L.

4.6.6 Comparator latch

The conventional latch show in Fig.4.19 used to latch the comparator output is sized with the minimum transistor sizes for the NMOS and with the PMOS transistor widths roughly the double to obtain a similar rise and fall times. Those sizes were

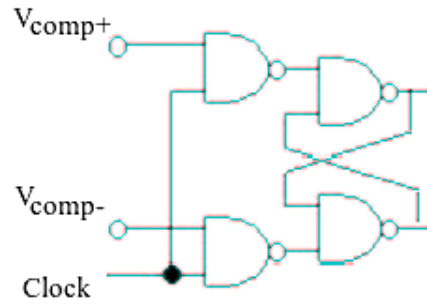


Figure 4.19: Comparator latch.

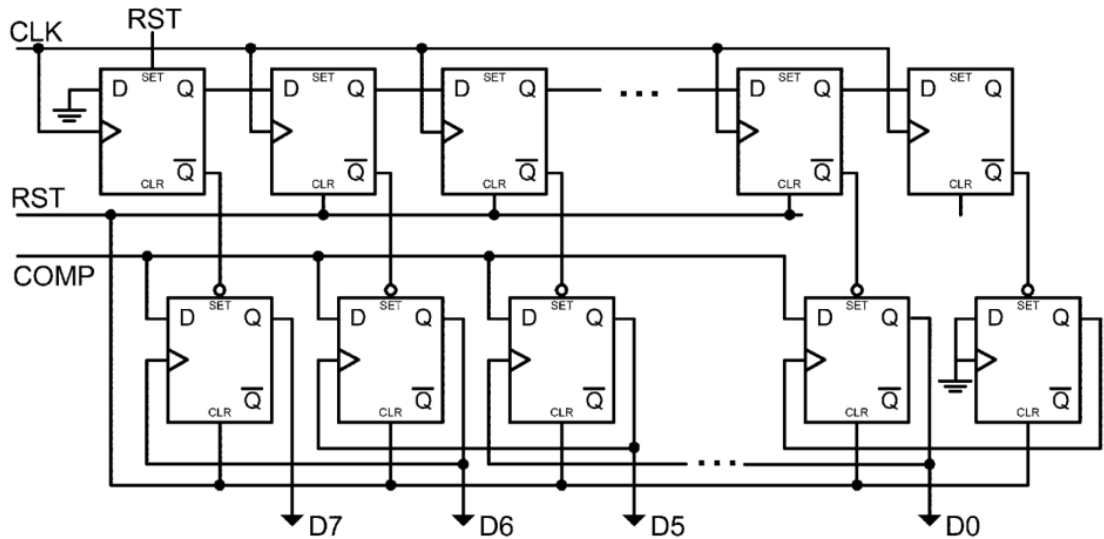


Figure 4.20: Simplest realization of the digital control as an LFSR [1]

in low frequency suitable for the desired operation in favor of minimizing power consumption.

4.7 SAR Control Logic

A sequential finite state machine (FSM) can be used in the conversion as shown in table 4.7 to realize the SAR algorithm used with the single-ended double-reference 8-bit architecture

Fig. 4.20 similar to [1] shows the simple direct realization of the SAR logic control, using $2(N + 1)$ D-flipflops Where N is the ADC resolution. All the D-flipflops RESET ports are connected to the RST signal except for the first one which has its

Table 4.1: SAR control logic.

Step	Input DAC signal								Comp o/p
0	0	0	0	0	0	0	0	0	N/A
1	1	0	0	0	0	0	0	0	a7
2	a7	1	0	0	0	0	0	0	a6
3	a7	a6	1	0	0	0	0	0	a5
4	a7	a6	a5	1	0	0	0	0	a4
5	a7	a6	a5	a4	1	0	0	0	a3
6	a7	a6	a5	a4	a3	1	0	0	a2
7	a7	a6	a5	a4	a3	a2	1	0	a1
8	a7	a6	a5	a4	a3	a2	a1	1	a0
R	a7	a6	a5	a4	a3	a2	a1	a0	N/A

input connected to '0' and its SET port to the RST signal while the RESET port is unconnected. The Lower flipflops SET ports are connected to the complementary outputs of the Upper flipflops after inversion with the clock port of each of them connected to the output of the next stage. The initial state all the outputs and the digital control bits is '0'.

With the RST signal arriving all the D-flipflops are still in the reset phase with output '0', except for the first D-flipflop where the RST signal is connected to its SET port. The output Q of the first D-flipflop is set then to '1' and its complementary output is set to '0' setting the first lower D-FlipFlop output D0 to '1' not caring for the comparator output, this is the operation of connecting the largest DAC capacitor to V_{ref} . At the next clock, RST signal returns low, the First upper D-flipflop changes output to '0' and the '1' spreads to the output of the second upper D-flipflop setting the second lower flipflop and D1 to '1' (next largest capacitor is connected to V_{ref}).

At this step the first lower flipflop has ended the SET phase and the first comparison also has ended. The action of setting D1 to '1' will trigger the first Lower flipflop to check the comparator output connected to its D terminal. According to the comparator output, D0 is kept '1' if the comparator output is '1' or changes to '0' if the comparator output is '0'. No more change will happen to D0 till end of conversion since its only triggered by the rising edge on D1. The operation then continues till all digits are ready and at the next RST signal, the digital output is read and stored and all D-flipflops are reset again.

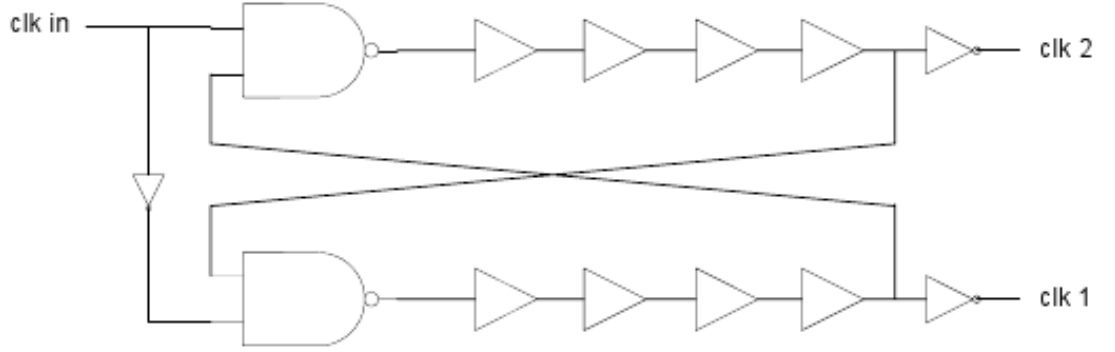


Figure 4.21: Non overlapping clocks generator.

4.8 Non-Overlapped Clock Generator

The control of the comparator, the DAC and the SAR block is based on the idea that some of these blocks is going to operate during the low state of the clock, while they are implemented with NMOS transistors that will need a positive input for operation. It's also very important that no overlap happens in the operation of those blocks to avoid leakage of DAC charge or an erroneous comparator decision. The generation of a 2 non-overlapped clocks is based on the circuit in Fig. 4.21 [38] The propagation delay of each inverter is found as:

$$t_p = \frac{C_L \cdot L}{2V_{dd}} \left[\frac{1}{K_p W_p} + \frac{1}{K_n W_n} \right] \quad (4.26)$$

Where C_L is the load capacitance at the output of each inverter, L is the length of transistor (the same for N and P transistors), W_p and W_n are the corresponding widths for P and N transistors of each inverter. A chain of symmetrical inverters is used on both branches to have a similar t_{d1} t_{d2} as shown in Fig. 4.22. The number of the inverters in the chain and their sizes determine the duration of non-overlap.

4.9 Conclusion

In this Chapter all the successive approximation circuit level blocks were presented, binary-weighted DAC architectures are preferred because they are relatively having wider margins for upper plate and routing parasitics. The minimum allowed unit capacitance is limited by thermal noise and capacitor mismatch margins while the maximum value is limited by the sampling frequency. MIM capacitors were presented as a good candidate in terms of linearity, area and parasitics. Special bootstrap switch was modified and used to solve the leakage problem in single-ended double-reference architectures while maintaining adequate reliability. The comparator circuit sizing trade-offs were analyzed. Finally, a simple SAR algorithm

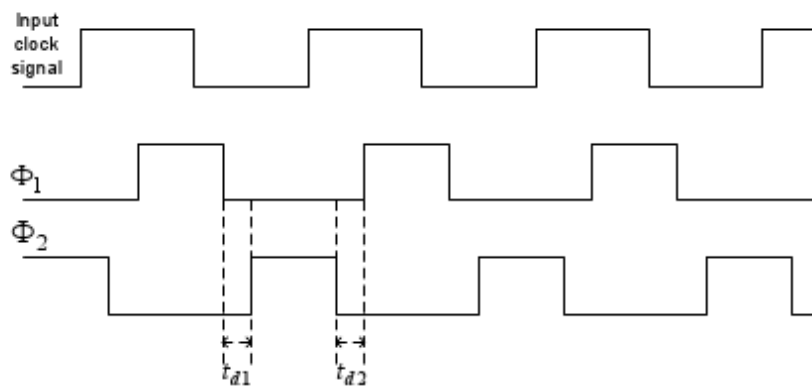


Figure 4.22: Non overlapped clocks.

implementation for single-ended architecture in digital gates is illustrated.

Design Automation

5.1 Introduction

In this Chapter, the systematic design methodology for successive approximation ADC is presented in section 5.2. Then it is explained in details: the system level design in section 5.3, the circuit level design in section 5.4 and the layout generation method is explained in section 5.5. Design automation techniques are exploited. At the circuit level, COMDIAC "COMpilateur des Dispositifs ACTifs" is introduced for the comparator synthesis. At the layout level, CAIRO "Creating Analog IPs Reusable and Optimized" layout language is introduced. A special algorithm is used in the DACs floorplaning for an optimized unit-capacitance common-centroid-based layout. Design automation results are then presented and discussed.

5.2 Systematic Design Methodology

Successive approximation ADC systematic design methodology from system specifications to layout. is illustrated in Fig. 5.1. In this flowchart, the design process can be divided into three major parts:

- System level design.
- Circuit level design.
- Layout level design.

In the system level, the target specifications are the bandwidth, the resolution, the technology and the application power consumption margins. The system level design directly depends on the target specifications. The SA architecture, algorithm, DAC topology and sampling technique are selected. The clock frequency is selected according to the bandwidth and resolution. The thermal noise and component mismatch estimations for the selected architecture are calculated. According to these calculations, one or more clock cycles are assigned for sampling to guarantee the accuracy. The comparator specifications are defined according to the clock frequency, the common mode from the DAC, the supply voltage and the ADC resolution.

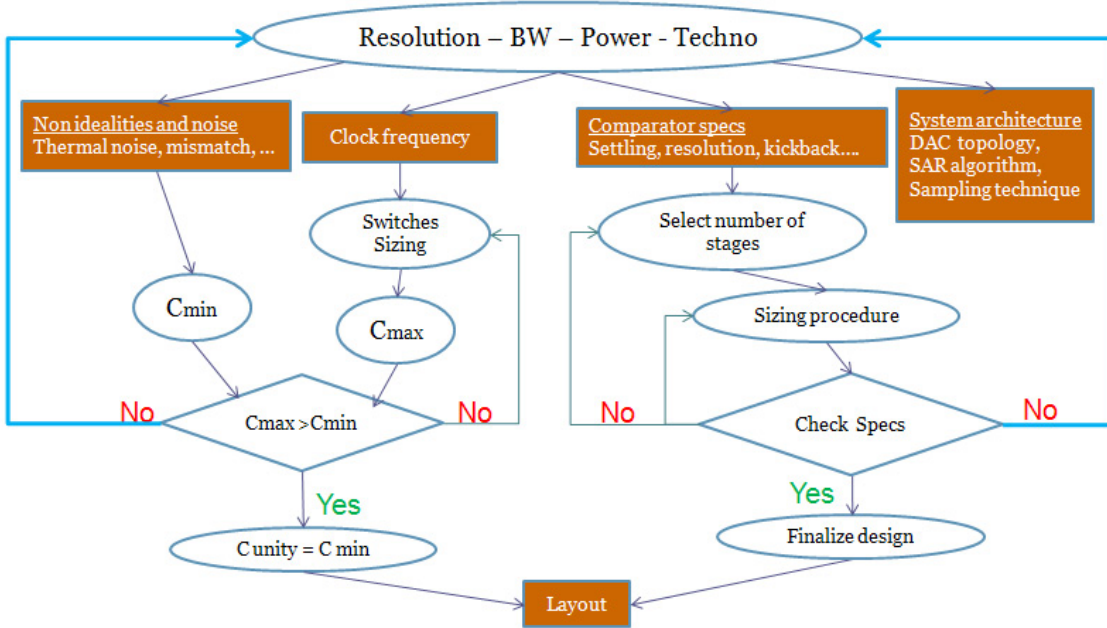


Figure 5.1: SA-ADC Design methodology.

In the circuit level design, the switches are sized as minimal size. The unit capacitance's minimum and maximum values that were calculated are checked; in case of infeasibility either the switches are resized for decreasing their resistance or system design specifications are relaxed.

The comparator sizing is based on the comparator specifications imposed in the system level such as resolution, settling time, offset and the effect of kickback noise on the DAC. The number of stages is selected and a sizing procedure is first tried. If the specifications are not met we may increase the number of stages, change the transistor sizes to improve both gain and decision time or relax the system specifications.

At the end, the unit capacitance is selected as minimum as possible and the comparator sizes are determined. The layout generation and the verification cycle follows.

5.3 System Level Design

5.3.1 Application Requirements

A double-reference single-ended architecture is recommended for very low-voltage low-power applications while a triple-reference differential architecture is recommended for high speed applications. DAC topologies like the reconfigurable-radix and the attenuator method can be used for reducing the area and increasing the operating frequencies on the expense of layout complexity and parasitics sensitivity. The sampling method for very-low-voltage applications is recommended through the

upper plates to use a minimum of special low-voltage switches.

5.3.2 Noise Budget

In order to achieve the target SNR, different non-idealities and noise sources discussed in Chapter 4 are studied. The corresponding total noise budget is allocated to guarantee the desired SNR. Ideally, with only quantization noise considered and for a sinusoidal input:

$$SNR = \frac{P_{sig}}{\Delta^2/12} \quad (5.1)$$

Allowing an increase of noise power of 50 percent as a noise budget for all noise sources and non idealities yields:

$$V_{n,budget}^2 = \frac{V_{FS}^2}{2 \cdot 12 \cdot V_{LSB}^2} \quad (5.2)$$

The noise budget allocated for all blocks

$$V_{n,budget}^2 \geq V_{n,KT/C}^2 + V_{n,comparator}^2 + V_{n,cap-mismatch}^2 \quad (5.3)$$

So for an 8-bit ADC, the theoretical SNR is about 43.8 dB from:

$$SNR = 6.02 \cdot N + 1.78 \quad (5.4)$$

Assuming 1.8 dB is acceptable as noise budget, giving a target SNR of 42 dB which will give the following noise budget:

$$V_n = \frac{V_{in,p-p}}{2\sqrt{2} \cdot 2^{43.8/20}} \quad (5.5)$$

5.3.3 Clocks and SAR algorithm

In this step, the SAR algorithm needed to control the ADC is written, the needed clocks for system control are defined (usually 2 non overlapped clocks). The clock frequency necessary to meet the specifications is selected with the usual initial guess $(N+1) \cdot 2 \cdot BW$. This assumes that the first clock is enough for sampling and inverting phases then N clocks for bit cycling. If one clock cycle is not sufficient for sampling, this can be arranged at the circuit level with reduced capacitance and switch resistances or at the system level by allowing more clock cycles for the sampling operation. For a target sampling frequency this will raise the clock frequency and sharpen the comparator specs.

An illustration of the differential architecture clock operations is shown in Fig. 5.2, where the first rising edge of ϕ_1 is for sampling, the first rising edge of ϕ_2 for inverting. A major precaution is to prevent the comparison phase to start during the DAC transients. This may lead to considerable errors limiting the ADC resolution.

The comparison phase starts at the falling edges of ϕ_2 . The digital latch regenerates the comparator outputs to the corresponding digital levels at the falling edge of ϕ_1 leaving enough settling time for the comparator outputs. It is assumed that the latched comparator gives enough gain to the compared signal levels, thus the time needed for the latch to regenerate digital output levels is almost negligible. So the digital latch is turned-on during the short period of non-overlap between ϕ_1 and ϕ_2 . The control logic receives the latch output at the rising edge of ϕ_2 and takes the switching decision for the DAC output. Then the cycle goes on till the new sampling signal arrives and the digital output is ready to read at this instant.

5.3.4 Consumed Energy

The consumed energy estimation for the DAC and the switching logic during a complete conversion is stated in [31].

$$E_{DAC} = \eta 2^N C_0 V_{dd}^2 \quad (5.6)$$

Where C_0 is the unit capacitance and η is a factor modeling the dependence of the total energy drawn on V_{in} , a value of 0.7 is a reasonable approximation for η according to [39], Eq. 5.6 shows that the unit capacitance is to be kept as low as possible in power-efficient applications. The DAC power consumption is derived for a binary weighted DAC and stands for differential and single ended implementations. The DAC consumption per conversion step is averaged by

$$P_{DAC} = \frac{\eta \cdot f_{sampling} \cdot 2^N C_0 V_{dd}^2}{N} \quad (5.7)$$

Then the total energy consumed by the comparator during a complete conversion including the latch contribution

$$E_{comp} = \frac{N}{f_{sampling}} I_{comp} V_{dd} + N C_{latch} V_{dd}^2 \quad (5.8)$$

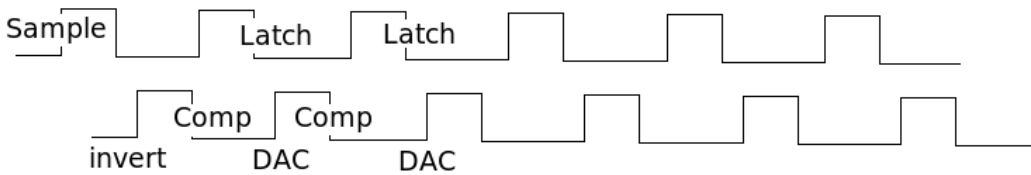


Figure 5.2: Clocks needed and overview of the SAR timing steps.

Where N is the number of bits, I_{comp} is the total biasing current in both branches of the comparator and C_{latch} is the total capacitance at the latch output nodes. The comparator draws current only during half the clock period, the comparator power consumption per conversion-step is then given by

$$P_{comp} = \frac{1}{2}(I_{comp}V_{dd} + C_{latch}V_{dd}^2f_{sampling}) \quad (5.9)$$

At low resolutions, the control logic energy dominates and the energy grows linearly with N ; at moderate resolution, the comparator begins to dominate and at high resolutions (more than 8 bits), the DAC energy becomes the dominant. The energy consumed by the control logic will be neglected through this analysis.

5.4 Circuit Level Design

5.4.1 Unit Capacitance

The factors considered in the unit capacitance selection were discussed in Chapter 4. The thermal noise and mismatch impose a lower limit for the unit capacitance selection while the sampling frequency defines the upper limit margin. The expected worst case linearity error occurs at the MSB transition, with a ratio error of

$$\frac{\Delta C}{C} = \frac{1}{\sqrt{2^{b-1}}} \frac{\Delta C_0}{C_0} \quad (5.10)$$

Where ΔC_0 represents the standard deviation of the unit capacitance. It is required to maintain this error below the level of the least significant bit (LSB) imposing the second lower boundary for the value of the unit capacitance $C_{u,min,mismatch}$. Then the minimum capacitance allowed by the target technology is checked and the final minimum value is

$$C_{u,min} = \max(C_{u,min,mismatch}, C_{u,min,thermal}, C_{u,min,techno}) \quad (5.11)$$

Normally substituting for kT/C values, it is found that values of unit capacitance can be down to 10fF with the thermal noise still below $0.1 V_n$. This was also reported in the literature [1]-[16]. The kT/C noise is not limiting a binary weighted structure of a SA-ADC. Next, $C_{u,max}$ boundary is set by the value of the sampling circuit time constant from Eq. 4.12 $\tau = R_{eq} \cdot C_{total}$ such that:

$$\frac{T_{clk}}{2} > 3\tau \quad (5.12)$$

If $C_{u,max} > C_{u,min}$, the unit capacitance is selected minimum else a relaxation of the specifications is necessary.

5.4.2 Switch Sizing

An interesting and general sizing methodology for switches is used in [11] taking in consideration for more accuracy the switches that may start conduction in the saturation region. Neglecting this fraction of time and considering only the switch is always conducting in the linear region, thus for a given allowed error ϵ and a settling time t_{lin} ,

$$t_{lin} = \tau \ln\left(\frac{1}{\epsilon}\right) \quad (5.13)$$

$$t_{lin} = (R_{switches,bottom} + R_{switch,top})C_{total} \cdot \ln\left(\frac{1}{\epsilon}\right) \quad (5.14)$$

Starting by a minimum size switch W_{min} and L_{min} the resulting time constant of the switches R_{on} and the total DAC capacitance are checked with the allowed error ϵ and settling time t_{lin} . For low frequency applications switches parasitics are not degrading performance and large switch sizes may be selected to reduce the switch resistance if the total capacitance is larger than the settling requirements.

5.4.3 Comparator Sizing Approach

5.4.3.1 Automatic Analog Synthesis

The circuit sizing environment COMDIAC [10] is a knowledge-based approach, it stands for "COMpileur des Dispositifs ACTifs". COMDIAC facilitates the capture of circuit sizing knowledge in the form of guided design plans. The tool is essentially composed of a set of C functions that allow the designer to accurately calculate different device parameters. For example, given transistor bias voltages, drain-source current and channel length, COMDIAC supplies the transistor width and all small-signal parameters. Using those functions, routines developed for basic sub-circuits sizing can be used in a hierarchical manner. For example, a differential pair is handled as an entity which contains two identical common-source transistors and a biasing current source.

This hierarchical approach simplifies the addition of new topologies by reusing specific design knowledge. Choosing a particular fabrication process is completely decoupled from the sizing procedure itself, such that the same circuit can be easily sized in multiple fabrication processes using different transistor models. Advanced transistor model equations like BSIM3V3 and MM9 as well as traditional SPICE MOS levels 1, 2 and 3 are incorporated in the tool. In addition, based on these equations, a guided user interface allows the designer to easily characterize different technologies by plotting transistor small signal parameters such as transconductances and capacitances with different bias voltages, transistor sizes and operating temperatures. This helps the designer to choose the most suitable fabrication process for a given application.

The philosophy of sizing plans in COMDIAC is to focus on the most significant performance characteristics while leaving the possibility to the designer to control

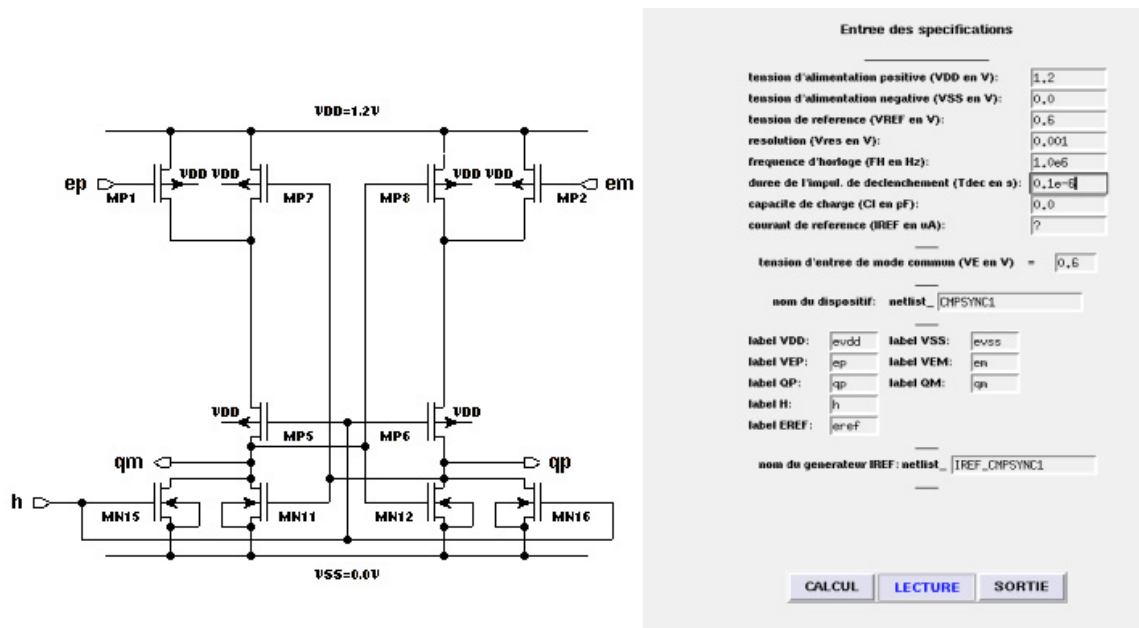


Figure 5.3: OCEANE schematic template with input parameters.

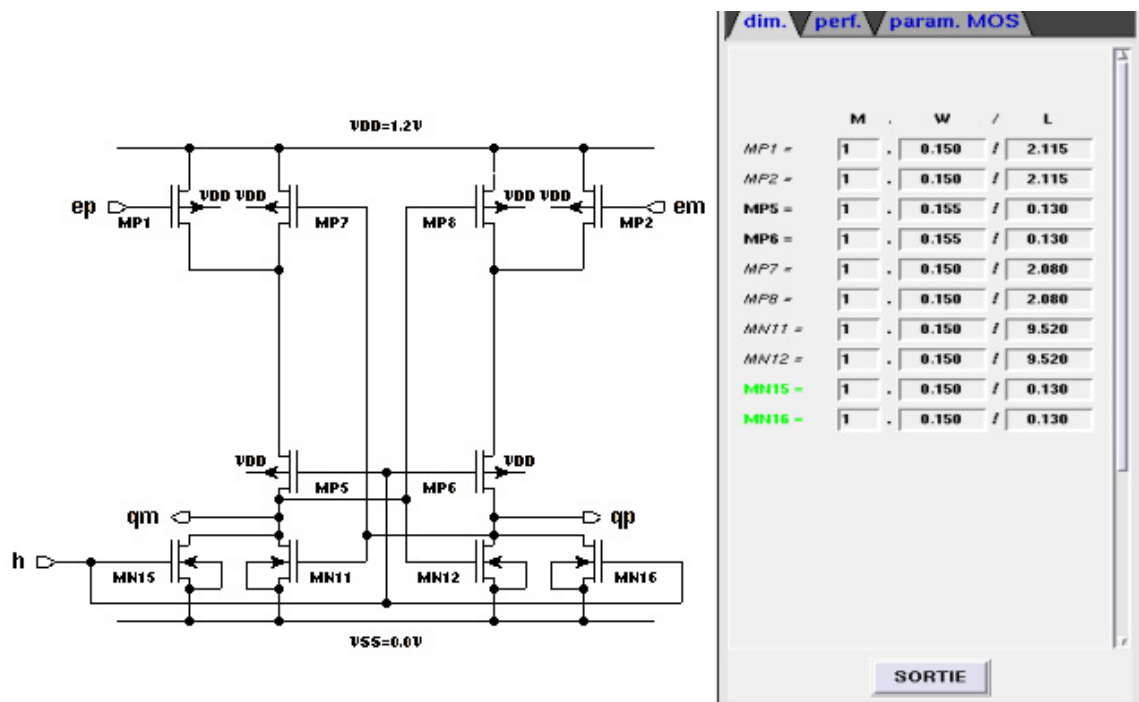


Figure 5.4: OCEANE generated comparator sizes.

interactively design details, thanks to a fast and accurate performance evaluation based on pre-derived equations that are defined by the design plan. The tool is very flexible and offers multi level of abstraction. It can receive from the user the process parameters; the transistor type (N or P) and the layout style which includes the number of fingers, number of shared source and drain diffusions between fingers and drain/source diffusion width.

5.4.3.2 Comparator Design Trade-offs

In order to understand the automation key Equations, we recall that the operation of the comparator has been introduced as 3 phases:

- Static gain by the input pair to turn on the latch during time T_{init}
- Dynamic gain till the latch feedback gain becomes positive at instant T_z
- Latching the outputs T_{latch}

The comparator response time is dominated by T_{init} and T_{latch} , so while T_z may be neglected to simplify the analysis. The period T_{init} decreases when increasing current and decreasing C_{init} which can be achieved by reducing L as possible.

$$T_{init} \approx \frac{C_{init} V_{th,M1}}{I_{ds,M1}} \quad (5.15)$$

$$T_{latch} = \frac{\tau_L}{A_0 - 1} \cdot \ln \frac{V_{FS}}{V_{res}} \quad (5.16)$$

It is required that the sum of the two phases becomes less than half of the clock period needed for a comparator decision and settling.

$$T_{init} + T_{reg} < T_{clk}/2 \quad (5.17)$$

Selecting the transistor dimensions is summarized in the flowchart of Fig. 5.5, to minimize T_{init} and T_{latch} it is required to increase the current. But increasing the area will increase parasitics so C_{init} and C_{latch} , decreasing L can make a good compromise between both requirements. For reducing offset and for independence of the load capacitance, it is required to increase area while its independent from W/L ratio. The forth parameter is the low power consumption which implies decreasing current. Increasing L will be a good solution for both requirements. At the end a trade-off between increasing L and decreasing L to achieve the demanded comparator specifications.

5.4.4 Comparator Latch

For the digital latch, only the T_{latch} is considered since the comparator outputs are assumed already near the digital levels. This latch stage needs relaxed V_{res} value. Decreasing the transistors areas while keeping W/L minimal will decrease C_{latch} and

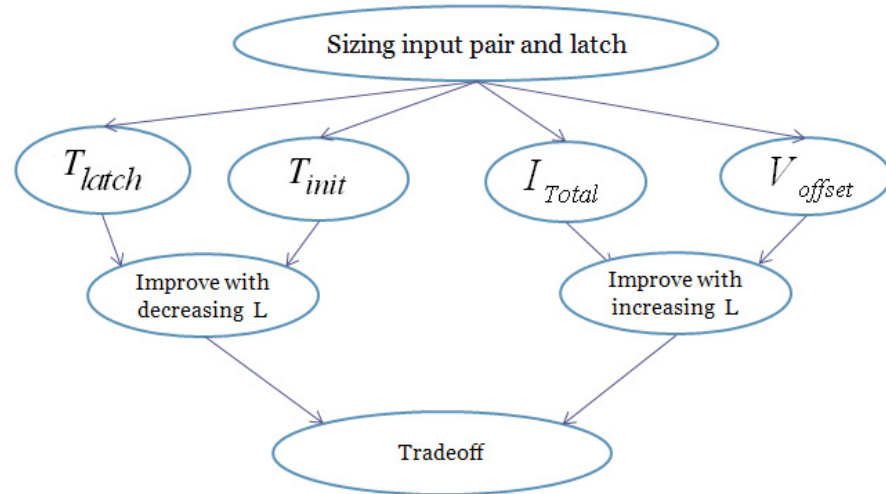


Figure 5.5: Comparator sizing methodology

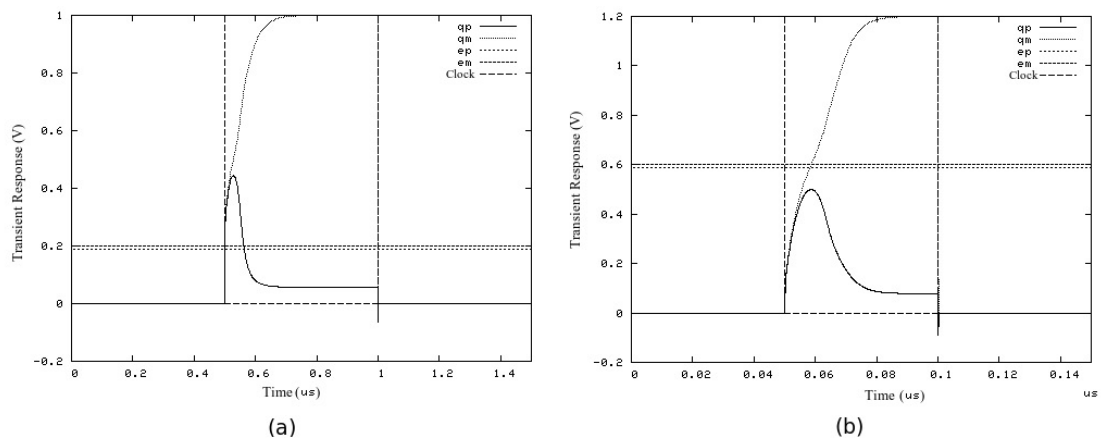
Figure 5.6: Comparator response time at 1MHz clock (a) Sized for current I_1 (b) Sized for current $I_2 > I_1$

Table 5.1: Mismatch Analysis for an 8-bit SA-ADC for several unit capacitance values The resulting SNDR is measured in dB.

C_u	Variance σ					Ideal
	0.01	0.02	0.05	0.1	0.2	
10fF	47.24	46.50	42.75	38.80	33.50	47.47
20fF	47.34	46.95	43.34	40.37	35.31	47.47
30fF	47.37	47.06	45.43	41.40	38.26	47.47

increase r_o , thus T_{latch} decreases. Minimal size transistors are recommended for this latch.

5.4.5 Mismatch Analysis

To check the mismatch effect of the DAC unit capacitances, A MATLAB program was written to add random error using a Guassian Distribution on each unit capacitance with a selectable variance (σ).

The generated values are passed to the Eldo netlists and the ADC performance is evaluated through the set of transient analysis, FFT processing and SNDR calculations to justify the selected unit capacitance value. The unit capacitance may be changed through several iterations until the estimated mismatch effect on the ADC performance becomes negligible.

A summary of the simulations set with mismatch for several values of unit capacitances and several variance (σ) values are tabulated in the following table.

5.5 CAIRO Layout Generation Philosophy

CAIRO stands for "Circuits Analogique Intgrs Rutilisables et Optimiss". It is a layout language that allows the designer to easily describe both relative placement and routing, and provides a set of predened device generators which are part of the language. CAIRO is implemented in the form of a documented superset of C functions. The language is constructed on top of a set of pre-existing functions (Genlib) for procedural layout that were successfully used in the ALLIANCE CAD System [LIP6] for the development of parameterized digital module generators.

CAIRO approach is classified as a knowledge-based approach and it relies on the following template definitions:

- Schematic template: defines a fixed circuit topology and connectivity for a given function, without any information on device sizes or component values (transistor W/L, capacitance value, . . .) which are considered as design parameters.

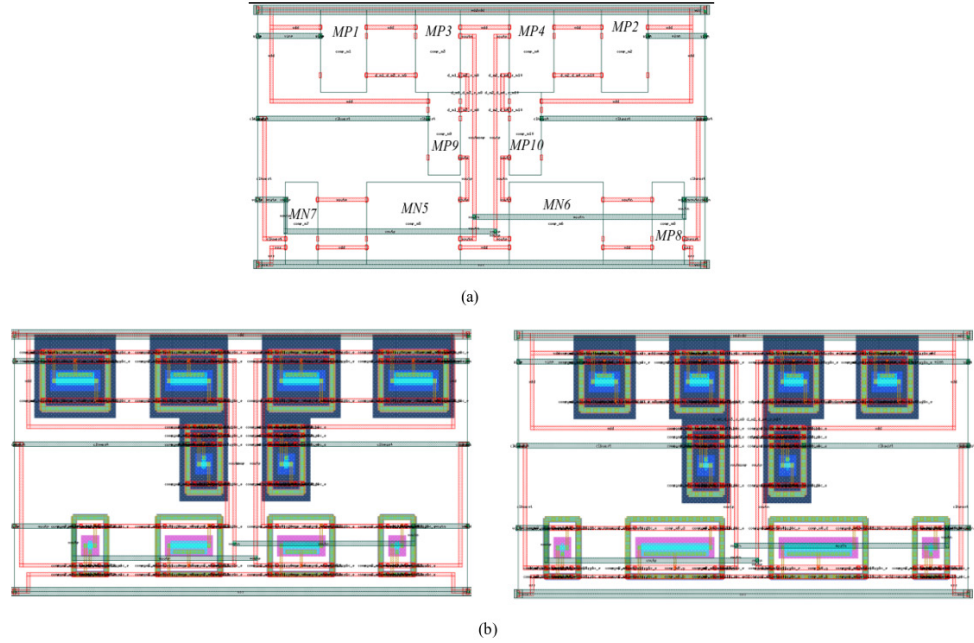


Figure 5.7: (a)CAIRO layout template example (floorplaning) (b) Generated layouts for different currents .

- Layout template: defines both physical device relative placement and relative routing paths for a given schematic template, without any information on component sizes or the final layout aspect ratio.

5.5.1 Comparator Layout

A CAIRO program was written to describe the comparator schematic and layout. Both the node connections and the desired floorplanning of the comparator transistors were described. This program offers a customizable technology independent template with the possibility of changing the layout design parameters without re-making the layout. For the comparator case, the layout design parameters are transistor sizes, fingers and dummies. The program receives the design parameters either manually or through automatic export from the sizing tool introduced in section 5.4.3.1.

5.5.2 Common Centroid Placement Algorithm

Since matching between unit capacitance was of major importance to reduce harmonic distortion. An optimized Common Centroid placement is used for the unit capacitance placement. This algorithm is written in C and it is first presented in [12]. Some changes were needed to extend its capacity to any number of unit capacitances. An example of common centroid placement is shown in Fig.5.8 for the

```

how many capacitors? 5
routing? 1
enter values
1 1 2 4 8
use rectangles?(1=yes)1
enter unit capacitor side length:
1
enter length:
4
sum:16
4      5      5      4
5      2      3      5
5      3      1      5
4      5      5      4

```

Figure 5.8: Common centroid placement for 5 binary weighted capacitors.

simple single-ended double-reference 4-bit SA-ADC.

The program receives the number of capacitors, the desired matrix shape through the length X and width Y, the routing method whether horizontal or vertical, the unit capacitor side length and finally the desired matching method whether rectangle or circle based.

5.5.3 Automatic MIM-Matrix Routing

Routing such great numbers of unit capacitances placed in a common centroid symmetry is quite difficult. An automatic routing scheme for randomly placed unit capacitances is offered by the new experimental CAIRO library MIM-matrix. Another CAIRO program was written to call the placement algorithm and pass its results to the library MIM-matrix for routing. This library receives the unit capacitance value, the capacitors number and their ratios. An example for the automatic capacitor array routing is shown in Fig.5.9. The routing for k capacitors will use $k(k+1)$ vertical paths, each unit capacitance is tied to its corresponding paths, one for the upper plate and one for the bottom plate. There are k vertical paths on the upper and lower edges of the layout to collect those distributed capacitances top-plate and bottom-plate in parallel to form the k capacitors. For the required binary weighted DAC, the top plates of all DAC capacitors are tied together. Thus, the vertical upper paths should be shorted to form only 1 terminal for the DAC output to the comparator. The vertical lower paths represent k terminals corresponding to the k capacitors bottom plates. Fig. 5.10 shows the generated capacitor matrix layout for 3 capacitors.

Routing parasitics are expected to be high specially with all the DAC top-plates joined together, so another possible approach in order to minimize the routing parasitics is to eliminate unused tracks instead of having $k(k+1)$ vertical track. As example, the smallest capacitor that is made of only one unit capacitance does not

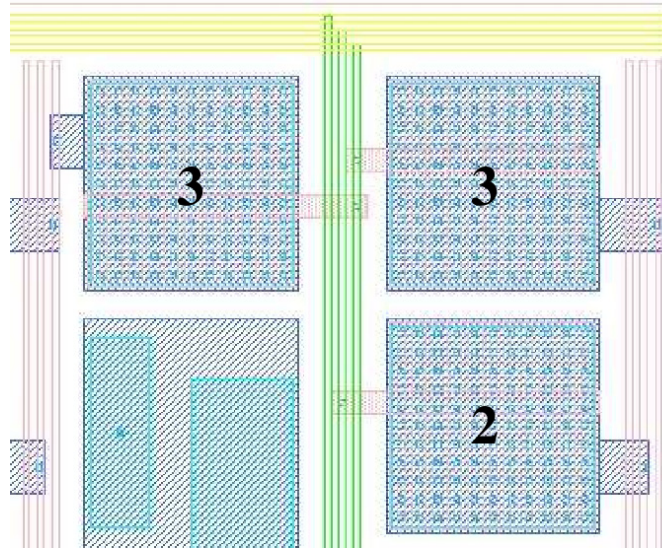


Figure 5.9: Close look on the capacitor matrix routing used in CAIRO MIM-matrix library.

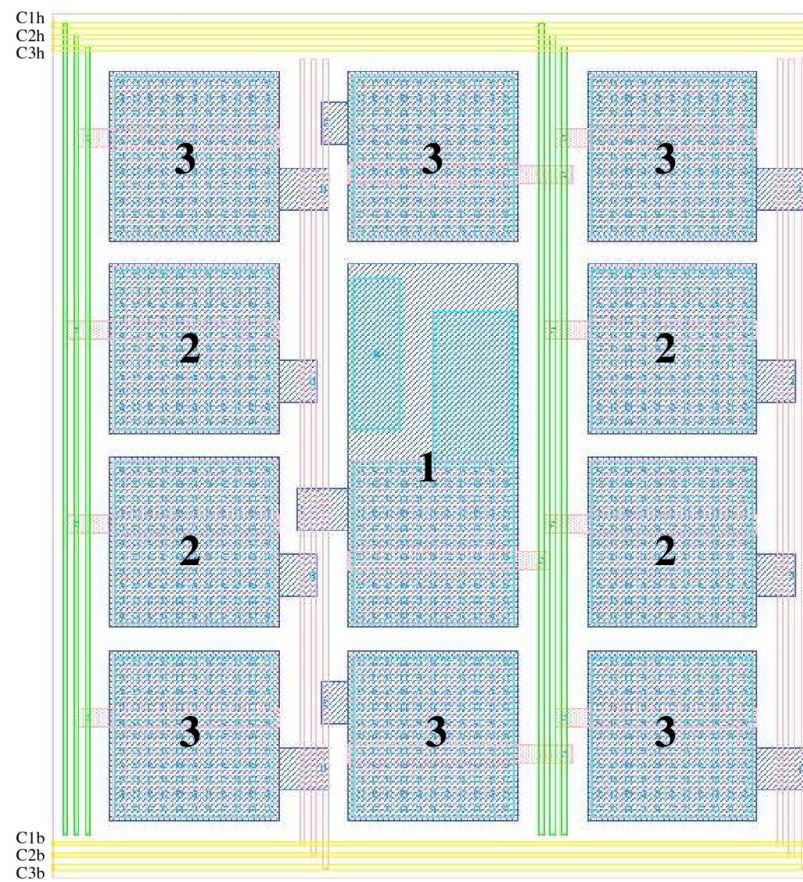


Figure 5.10: MIM matrix generation example for 3 capacitors with different ratios.

need to have a dedicated 2 vertical routing wires repeated $k+1$ times since already it needs only to use 2 wires. However, it is reported by [23] that with the DAC top plates parasitics up-to $100C_u$, the ADC accuracy is not affected. With the upper plates tied together Their corresponding parasitics are parallel and will represent simply an offset for the DAC that can be removed in the digital domain. While the bottom plate parasitics are not interfering with the DAC operation in the charge redistribution phase. The only remaining parasitics operation are the parasitics between the capacitors due to routing crosses. Optimizing the routing and the remove of unnecessary wires is necessary to minimize those inter-capacitor parasitics that may degrade the performance.

5.5.4 Complete Layout Generation

The comparator and the DAC layout templates are reusable for any technology according to CAIRO philosophy. Design parameters such as unit capacitance value or transistor sizes may be changed easily and the layout is reused and generated for the new technology or design parameters. For full SA-ADC reusable design, a CAIRO program is necessary to describe the ADC floorplan and the blocks connectivity. The switch array block layout generation is straightforward and no special layout techniques are needed. Through the hierarchical feature offered in CAIRO. This program will then instantiate the different CAIRO programs previously written for the layout description of

- The capacitive DAC(s)
- The latched comparator
- The switches array
- The bootstrap switches (for double-reference single-ended versions)
- The digital latch
- The SAR control logic
- The non-overlapped clocks generator

The results of the ADC floorplan are intended to be like [1] presented in Fig. 5.11.

5.5.5 Layout Verification

The layout plan and verification is summarized in the flow-chart of Fig. 5.12. The outputs of the design phase of section 5.2 are passed through layout templates to the layout generator where now combined with the target technology gives a GDS file which could be verified using any commercial EDA tool. The layouts are then exported to CADENCE to perform Design rule checks (DRC), Electrical rule checks

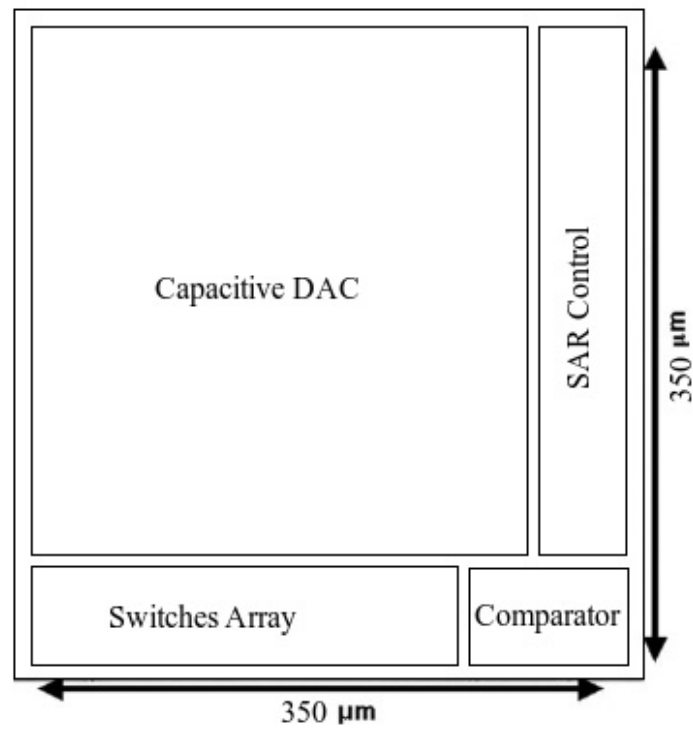


Figure 5.11: Target ADC floorplan.

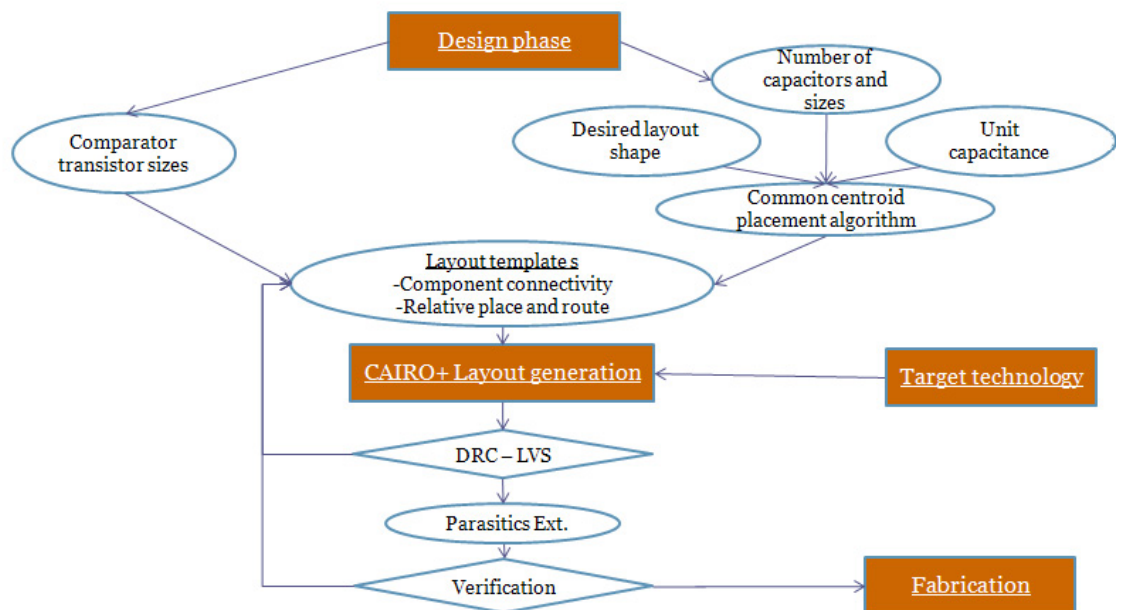


Figure 5.12: Layout generation and verification flow.

(ERC) and layout v.s. schematic check (LVS). For any problem in this level, the layout templates have to be checked for connectivity problems since normally CAIRO prevents DRC errors. At last a netlist is extracted with parasitics and again a set of transistor level simulations are to be run to characterize the expected ADC performance with parasitics. In case of unacceptable parasitics values degrading the ADC performance, several iterations may be necessary regarding the layout template description, routing and the unit capacitance value.

5.6 Conclusion

In this Chapter, the design flow for the successive approximation ADC was presented, followed by system level design and circuit level parameters. The proposed systematic methodology makes use of novel analog design automation and reuse techniques. The analog devices synthesizer COMDIAC philosophy was presented and comparator simulation results for several specifications were presented. The Layout generation principle was introduced and layout templates were written in CAIRO to describe the different system blocks. The performance degradation shown in mismatch analysis was solved by a common centroid unit capacitance placement algorithm for any number and any weights of capacitors. The automatic routing for an arbitrary number of capacitors with random unit capacitances placement is offered through the MIM-matrix library. Finally the layout verification plan is presented, after exporting the generated layout to commercial EDA tools.

Case Study

6.1 Introduction

In the following sections a case study is presented using the design methodology presented in Chapter 5. The target specifications and technology are presented in section 6.2, then system architecture, circuit design parameters for all system blocks are discussed in section 6.3. COMDIAC results for the comparators design were shown then the verification plan and the transistor level simulations are presented in section 6.4, the system power consumption is calculated in section 6.3.3 and the layout considerations are explained in section 6.5. The layouts of the main system blocks are presented in sections 6.6, 6.7, 6.8 and 6.9. Finally section 6.10 summarizes the realized ADC results to compare with the state of the art.

6.2 Target specs

The proposed systematic design methodology in chapter 5 was used to design a successive approximation ADC with the required specifications for wireless sensor nodes [1] from the system specifications to transistor and layout levels

- Resolution (N): 8 bit
- Bandwidth (BW): 50 KHz
- Clock frequency (f_s): 1 MHz
- Technology: 0.13 μ m ST, 1P6M (1 Poly and 6 metal layers) with MIM capacitors
- Power: Minimize power consumption

6.3 System Architecture

Both single-ended double-reference and differential triple-reference implementations were designed. One clock cycle was reserved for sampling and inverting phases while

Table 6.1: Comparator transistor sizes for 8 bit resolution Differential SA-ADC.

	MP1	MP2	MP5	MP6	MP7	MP8	MN11	MN12	MN15	MN16
M	1	1	1	1	1	1	1	1	1	1
W (μm)	0.15	0.15	0.155	0.155	0.15	0.15	0.15	0.15	0.15	0.15
L (μm)	2.115	2.115	0.13	0.13	2.08	2.08	9.52	9.52	0.13	0.13

N cycles for the charge redistribution phase. The sampling rate is then $\approx 111KHz$ and the system Bandwidth $\approx 55KHz$.

6.3.1 Circuit Design Parameters

The thermal noise was previously stated as a non limiting factor in moderate resolutions SA-ADC. This was justified for the used technology and the demanded resolution. The minimum unit capacitance of the technology of $30fF$ was chosen. For such a value, mismatch analysis predicts 0.7 dB loss in the $SNDR_{max}$ for a random unit capacitances deviations from the nominal value with only 0.01 variance. The charge injection as predicted didn't show any limitations. This was justified by transistor level simulations and no need for charge injection cancellation schemes in the design. Special care is then demanded in Layout through the use of common centroid matched designs. Minimal size switches were used and their resistance was negligible at the target sampling frequency with the selected unit capacitance. No further iterations were needed in this design path.

6.3.2 Comparator Design

Next, the comparator is designed as a one stage classic latched-comparator to decrease power consumption. Two comparators were sized using COMDIAC for both the single-ended double-reference ADC and the differential triple-reference ADC. This is due to the difference of the input transistors biasing for each case. The comparator used in the single-ended version is biased at V_{dd} but the one used in the differential version is biased at $V_{dd}/2$ due to the different SAR algorithms for both versions. A CMOS latch is used to give enough gain to shorten the latch time in the differential version while in the single-ended version only the normal positive feedback configuration was used. In both configurations the current is cut-off in the branches during the reset phase for lower power consumption.

The clock feed-through was negligible at the target frequencies and its value was always below $V_{LSB}/2$. The kickback noise was not limiting the DAC. The comparator resolution and settling time were adequate for the demanded specifications. The sizes for the designed comparators are in the following tables:

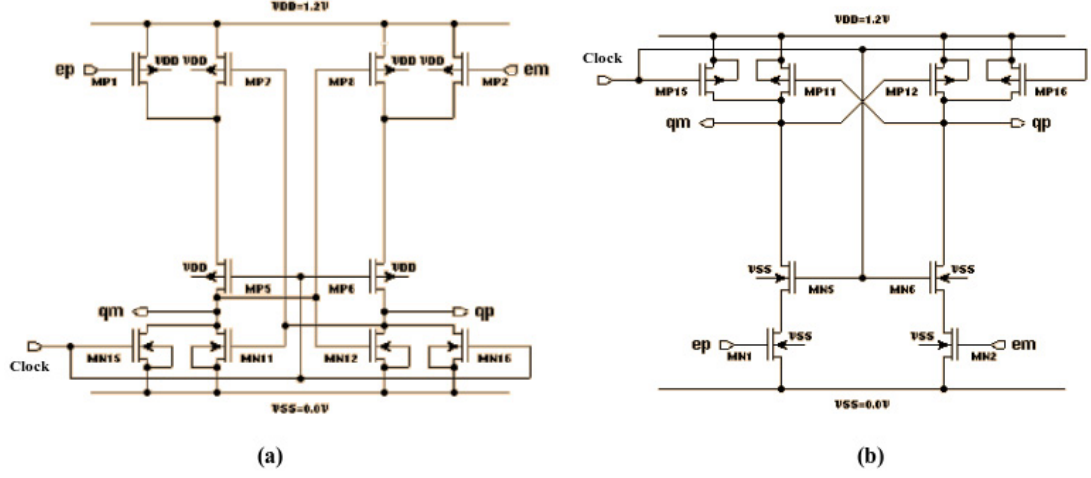


Figure 6.1: (a) Comparator for differential (b) Comparator for single-ended.

Table 6.2: Comparator transistor sizes for 8 bit resolution single-ended SA-ADC.

	MP1	MP2	MP5	MP6	MN11	MN12	MN15	MN16
M	1	1	1	1	1	1	1	1
W (μm)	0.15	0.15	0.315	0.315	00.15	00.15	0.15	0.15
L (μm)	2.80	2.80	0.130	0.130	10.12	10.12	0.13	0.13

6.3.3 Power Consumption

The Differential DACs consumption per conversion-step is calculated using Eq. 5.7, that will be repeated here

$$P_{DAC} = \frac{\eta \cdot f_{sampling} \cdot 2^N C_0 V_{dd}^2}{N} \quad (6.1)$$

While the comparator and latch consumption per conversion-step is

$$P_{comp} = \frac{1}{2} \left[I_{comp} V_{dd} + f_{sampling} C_{latch} V_{dd}^2 \right] \quad (6.2)$$

The dominant block with this sampling frequency and resolution is the comparator while the DACs and the latch have much less contribution. The total power consumed in a conversion is

$$P_{total} = N \cdot (P_{DAC} + P_{comp}) \quad (6.3)$$

The comparators for single-ended and differential implementations were designed for a $1 \mu A$ current, thus their energy consumption is the same. The DAC consumption is also the same for both. This is evident since the single-ended uses a double-reference

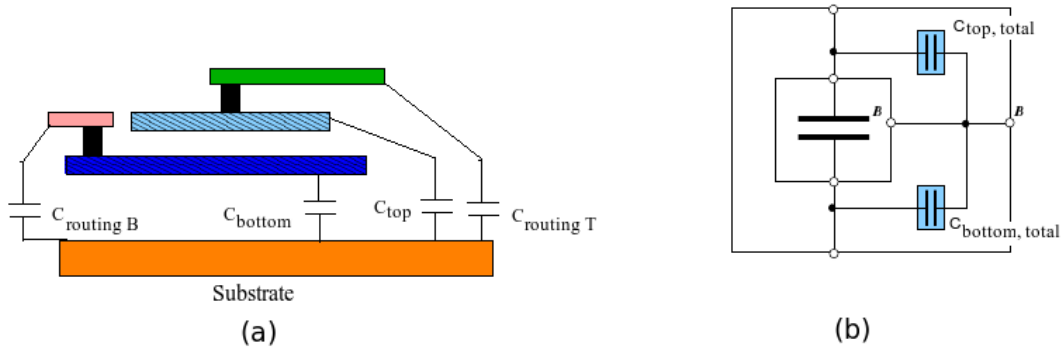


Figure 6.2: (a) MIM capacitor parasitics (b) CAIRO representation for the MIM model.

structure and the differential uses a triple reference. A triple-reference structure has half the total capacitance of the double reference for the same ADC resolution but a differential triple reference has a total capacitance equal to that of a single-ended double reference for the same resolution.

6.4 Verification

The multiple abstract simulation environment developed in VHDL-AMS was used for behavioral simulations, then for running transistor level simulations. Each time a block is replaced by its BSIM3 technology description to characterize non-idealities. The SAR algorithm is implemented in synthesisable VHDL. Eldo macro-models were used in the behavioral descriptions of the switches, the comparator, the digital latch, the non-overlapped clock generator and the DAC capacitors while models provided by ST 0.13 μm were used for the transistor level descriptions.

6.4.1 Models

The MIM capacitors model used in simulations considers the following parasitics contributions shown in Fig. 6.2 (a):

- the intrinsic capacitance between the top/bottom plate surfaces.
- the fringe contributions caused between the top plate sides and the bottom plate surface (C_{side} , C_{top} , C_{bottom}).

6.4.2 Verification Plan

A flow-chart for the verification plan is shown in Fig. 6.3 The binary weighted DAC topology, the SAR algorithm and the bottom plate sampling technique were all described in netlists. They are considered presets in the simulation environment. The

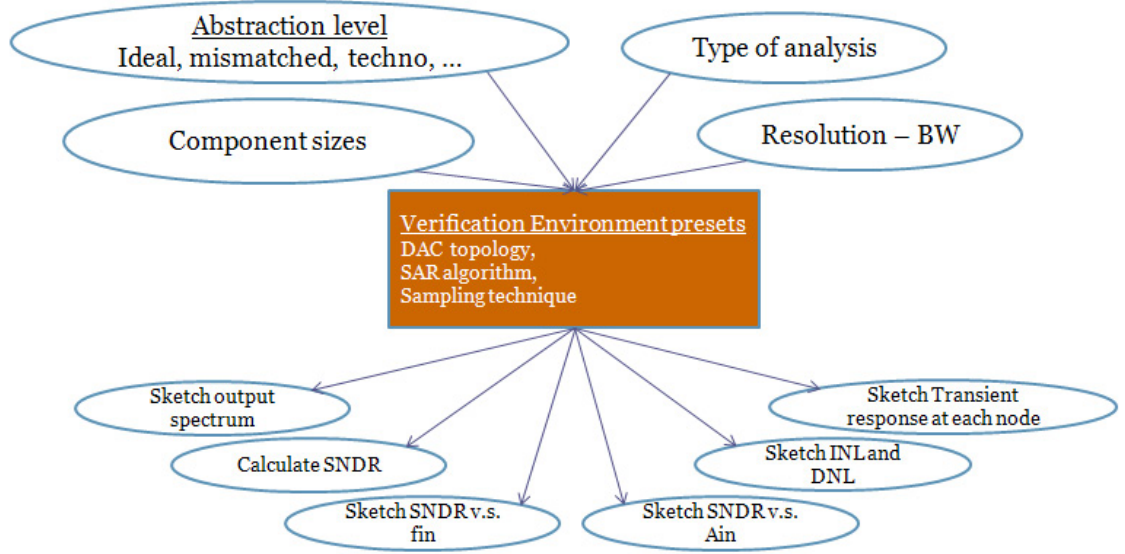


Figure 6.3: Verification plan realized by the developed multiple abstraction simulation environment

resolution, bandwidth, component sizes and the abstraction level are all customizable. The set of analysis used to characterize the performance of the designed ADC at all abstraction levels are

- Static performance
- Transient analysis
- Frequency analysis
- Tracing the $\text{SNR}-V_{in}$ curve
- Tracing the $\text{SNR}-f_{in}$ curve
- Comparing the results of the former analysis with those of the behavioral simulations
- Comparing the results with the stat of the art

6.4.3 Static Performance

Fig. 6.4 shows the ADC response in transient analysis for a slow ramp excitation with 16 samples per bin. This moderate number of samples per bin was chosen for reasonable simulation time with adequate accuracy for integral non-linearity (INL) and differential non-linearity (DNL) processing. The INL and DNL were analyzed and traced using a modified version of the MATLAB programs offered by [13] and both are below $V_{LSB}/2$. These values are within the accepted range predicted from theoretical analysis. The DNL definition used in the program is the end-point definition which removes offset and gain error in calculations.

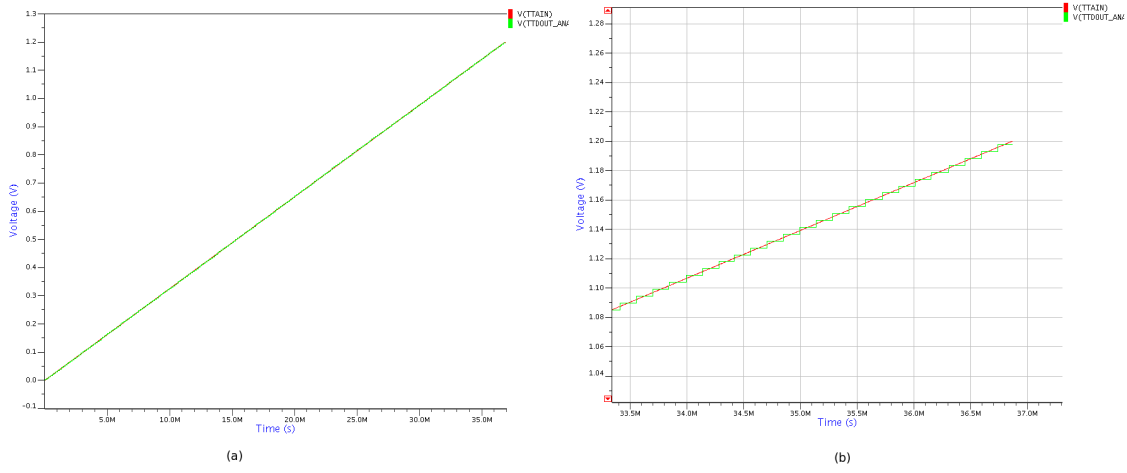


Figure 6.4: ADC response for a slow ramp (a) Full scale (b) zoom

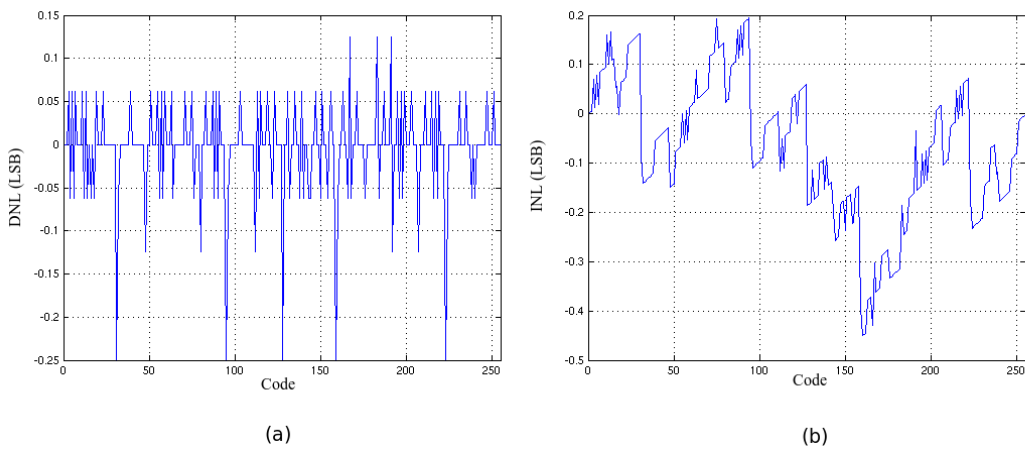


Figure 6.5: For 16 sample per bin measured in LSB (a) DNL (b) INL.

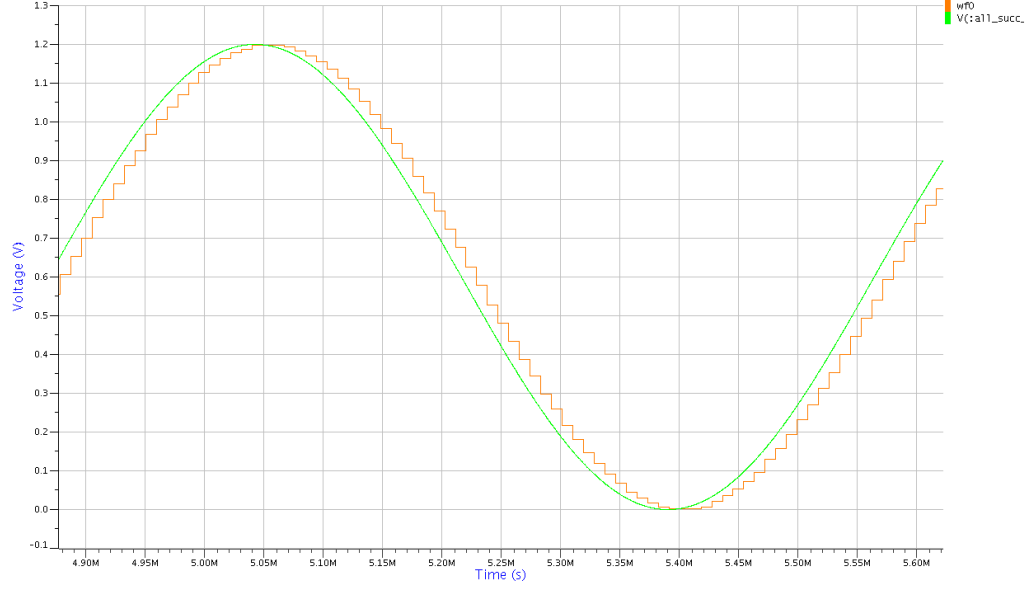


Figure 6.6: Time domain SA-ADC output coded in decimal with a full scale sinusoidal input.

6.4.4 Transient Analysis

The following figures show the outputs of the different blocks in transient analysis of the differential ADC. Fig 6.6 shows the time domain response of the transistor level SA-ADC. Performance of Differential and single-ended structures were almost the same. Differential DACs response for a full scale input sinusoidal is shown in Fig. 6.7 Fig 6.7 shows the output of the differential binary weighted DACs for a full scale sinusoidal input. During the conversion the DACs outputs clear the sampled input and return to $V_{dd}/2$ Fig. 6.8 shows The DACs outputs for a full conversion operation during 9 clock cycles. The comparison phase was carefully designed to start after the settling of the DACs transients to avoid wrong comparator latching during transients.

6.4.5 Frequency Analysis

The MATLAB program used to post-process the transient analysis results of the ADC output calculates the FFT using 4096 points and Blackman Harris window. The output spectrum for the output of the SA-ADC is shown for different level of abstraction. Fig. 6.9 (a) represents the spectrum and the SNDR for the ideal SA-ADC with behavioral description and ideal components. It is good in term of area to use minimum size if allowed because of the big number of switches used (≈ 64). In case of a single-ended architectures bootstrap switches also will use 22 additional transistors for solving the leakage problem while keeping the switches reliability. Fig. 6.9 (b) represents the results of replacing the ideal switches with minimal size

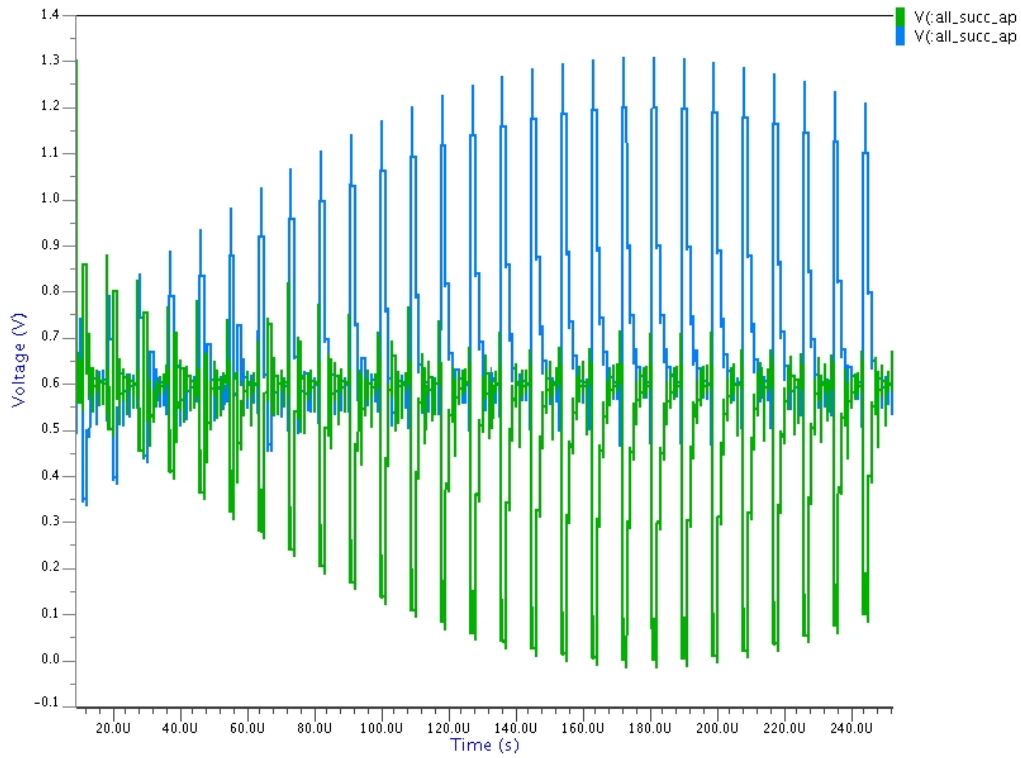


Figure 6.7: Differential DAC outputs for a full scale sinusoidal input.

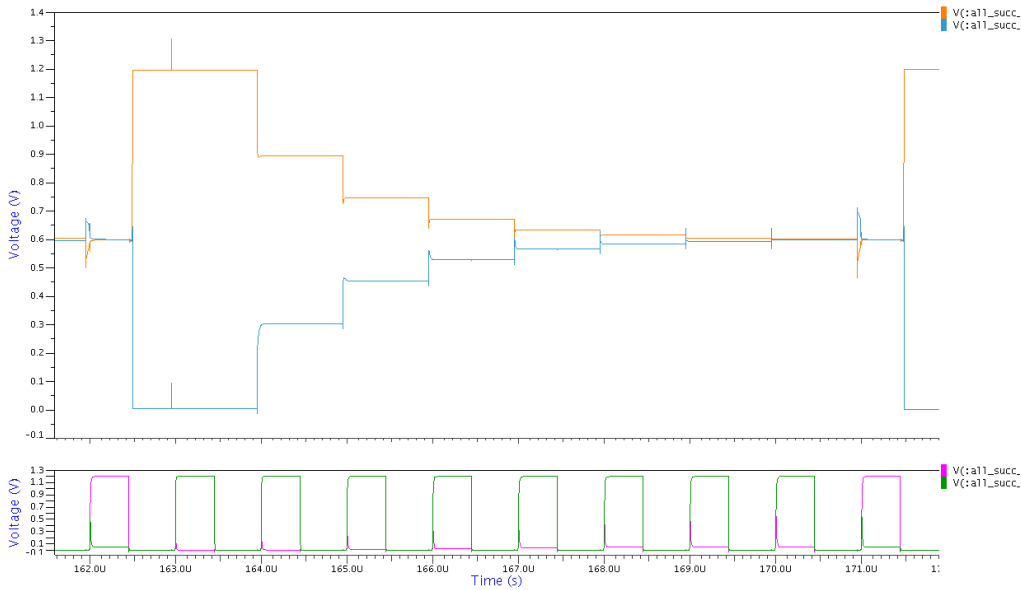


Figure 6.8: DACs outputs during the successive approximation operation and the corresponding comparator decisions.

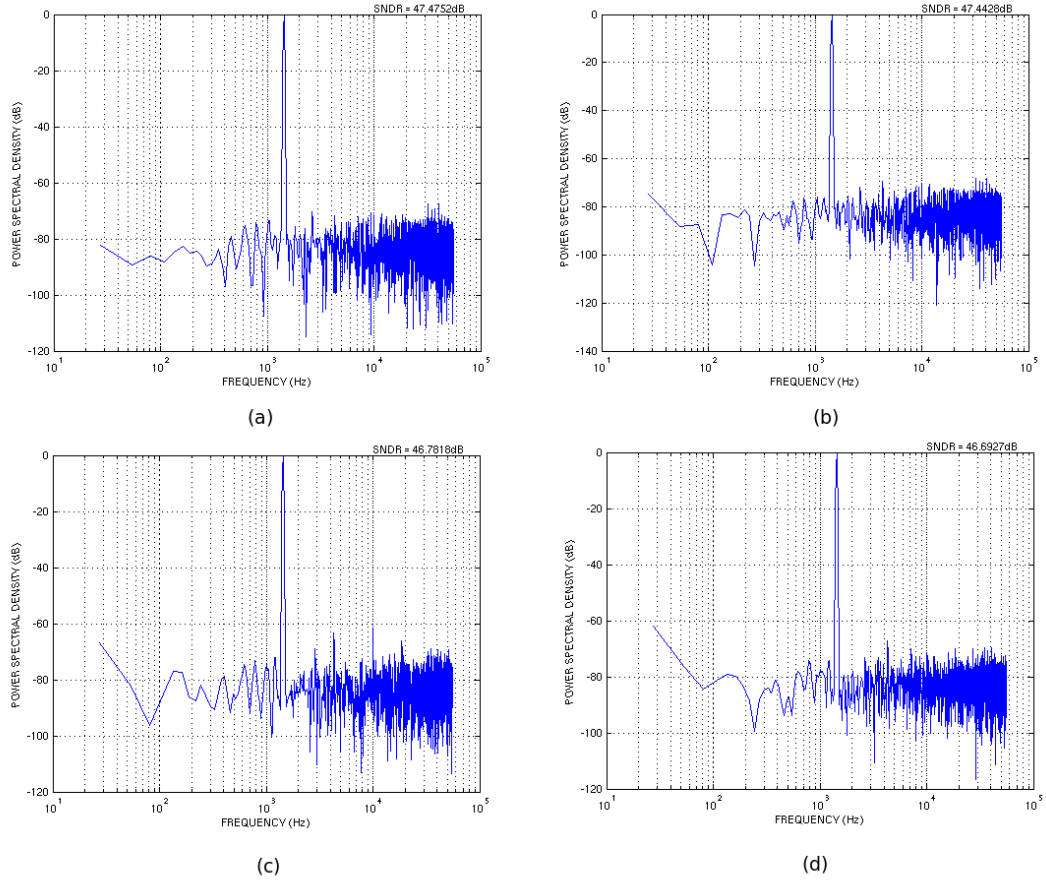


Figure 6.9: 4096 point FFT for the output spectrum (a) ideal (b) MOS switches (c) Mismatch with 0.01 variance on the unit capacitance (d) Latched MOS comparator.

BSIM3 models. No significant effect was noticed for this change. A random mismatch factor was added on each unit capacitance with 0.01 variance Fig. 6.9 (c) shows the corresponding changes in spectrum and SNDR. About 0.7 dB decrease in SNDR was detected and harmonics slightly begin to appear on the output frequency spectrum. Combining the mismatch with BSIM3 model descriptions for all blocks shows more degradation in the SNDR as shown in Fig. 6.9 (d).

6.5 Layout Considerations

The MIM capacitor as presented and discussed in section 4.4.3 uses dedicated metal layers in this technology. The technology offers the model of Fig. 6.2 and doesn't allow vias under the bottom plate of the capacitor. So routing of both plates is done through vias on the level of metal 6. A matrix of vias is used in unit capacitance connections for improving conductivity.

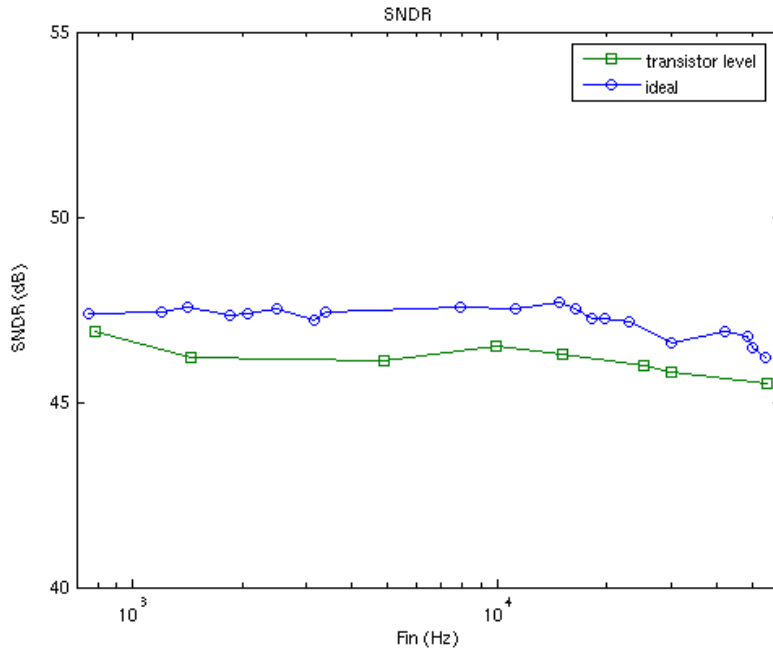


Figure 6.10: Maximum Signal to noise and distortion ratio SNDR v.s. Input frequency f_{in} upto the signal Bandwidth for transistor level and ideal models simulations.

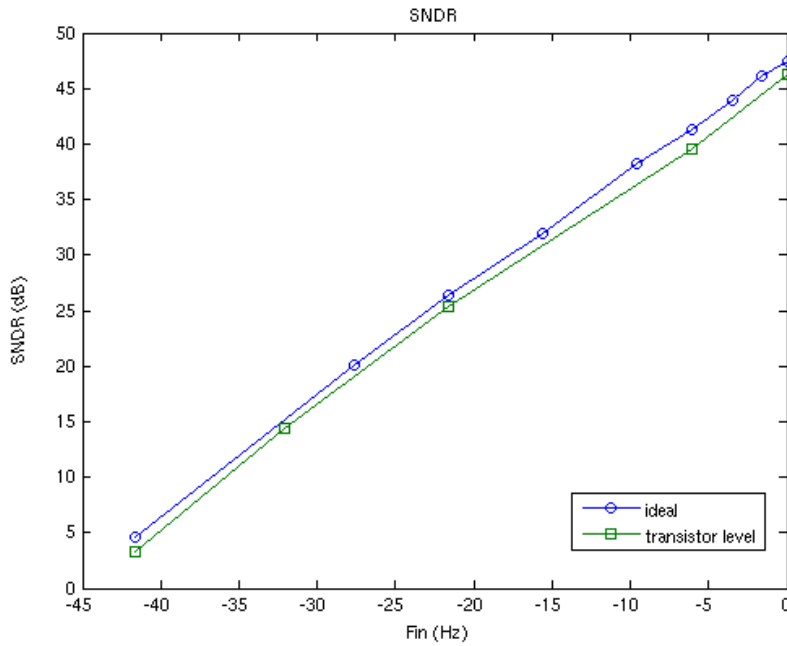


Figure 6.11: Signal to noise and distortion ratio SNDR v.s. Normalized input amplitude A_{in} from 0 to V_{FS} for transistor level and ideal models simulations.

6.5.1 Routing

Metal 1 and metal 2 are used for routing transistor level in the comparator, while metal 4 and metal 5 are used for power routing (V_{dd} and V_{gnd}) and inter-blocks (comparator, DACs, Switch array) connections were intended to be with metal 3. The layout drawn (for both the generated and manual layouts) have passed the Design rules and reliability rules check. The reliability rulebook determines the widths of metal layers and number of vias according to the value of the current flowing over them.

6.5.2 Dummies

The components at the extremities are susceptible to mismatches introduced in fabrication due to etching and shading effects. In order to ensure better matching between components, dummy devices are usually added to the design extremities [40]. Dummies were not used in these designs, though the feature does exist in CAIRO because the commercial EDA tools used in layout verification does not recognize the dummies generated by CAIRO. A modification of this feature is still under development.

6.6 Comparator Reusable CAIRO Layout

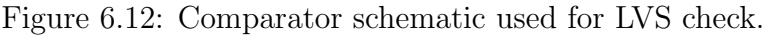
Comparator layout is generated by CAIRO after reading the necessary sizes of the transistors from COMDIAC. The layouts generated by CAIRO are not always optimum in terms of area, but the feature of technology portability with the same layout template and the customizable layout design parameters presents good advantages to the designer. The description in this layout template used a common centroid symmetry and the area is $22 \times 39 \mu m^2$.

The comparator layout GDS file was imported into CADENCE for layout verification, it passed Design rule check using CALIBRE and DIVA then layout versus schematic check using DIVA. Then the layout parasitics were extracted and used in post-layout simulations. No performance degradation was noticed.

6.7 Capacitors Common Centroid Placement

The MIM-matrix library of CAIRO offers an automatic routing for a capacitor array but it does not offer automatic placement, user has to write the values of the capacitors, the value of the unit capacitance and the desired placement for every unit capacitance and its corresponding capacitor.

The common centroid algorithm presented in section 5.5.2, implemented as a C program, is used with some modifications to increase the algorithm capacity for



```

how many capacitors? 16
routing? 1
enter values
1 1 1 1 2 2 4 4 8 8 16 16 32 32 64 64
use rectangles?(1=yes)1
enter unit capacitor side length:
1
enter length:
16
sum:256
16 16 15 15 15 15 16 11 11 16 15 15 15 15 16 16
16 16 16 16 11 14 13 12 12 13 14 11 16 16 16 16
15 16 14 15 16 15 13 16 16 13 15 16 15 14 16 15
15 16 15 12 14 15 13 16 16 13 15 14 12 15 16 15
15 11 16 14 14 15 14 13 13 14 15 14 14 16 11 15
15 14 15 15 15 9 10 12 12 9 10 15 15 15 14 15
16 13 13 13 14 10 8 5 6 8 9 14 13 13 13 16
11 12 16 16 13 9 7 2 3 7 10 13 16 16 12 11
11 12 16 16 13 10 7 4 1 7 9 13 16 16 12 11
16 13 13 13 14 9 8 6 5 8 10 14 13 13 13 16
15 14 15 15 15 10 9 12 12 10 9 15 15 15 14 15
15 11 16 14 14 15 14 13 13 14 15 14 14 16 11 15
15 16 15 12 14 15 13 16 16 13 15 14 12 15 16 15
15 16 14 15 16 15 13 16 16 13 15 16 15 14 16 15
16 16 16 16 11 14 13 12 12 13 14 11 16 16 16 16
16 16 15 15 15 15 16 11 11 16 15 15 15 15 16 16

```

Figure 6.14: DACs common centroid placement proposed for unit capacitances.

handling more than 300 unit capacitance.

The designed DACs are made of 256 unit capacitance constituting the 16 capacitors. Through the use of a shell script, the results of the automatic placement from the algorithm were automatically passed to CAIRO to call the MIM-matrix generator and generate the layout. The common centroid placement using rectangles is presented in Fig. 6.14.

6.8 DAC Reusable CAIRO Layout

The generated DACs layout from CAIRO is presented in Fig. 6.15 with full automatic routing. A close look on the routing is shown in Fig. 6.16. Several problems were met in verification due to a technology compatibility issue. The alu-cap layer which is a dedicated layer for the MIM upper and bottom plates is not recognized when converting to GDS file. This was manually corrected in the imported layout. Besides, the MIM-matrix generator had another problem in routing. It uses the capacitor bottom layer bot-mim and the alu-cap in routing. This was planned in order not to waste metals in intermediate capacitor routing in a small capacitor matrix. In cases with a big matrix with 256 unit capacitance this leads to the creation of huge parasitics. Every intersection of these layers in routing will create a considerable interconnect parasitics which was verified in parasitic extraction. Finally, the geometrical constraints imposed by DRC on those 2 layers which turns the matrix too wide. The routing uses most of the area and a 16x16 matrix turns out to be a large rectangle with area $1.262 \times 0.258 \text{ mm}^2$.

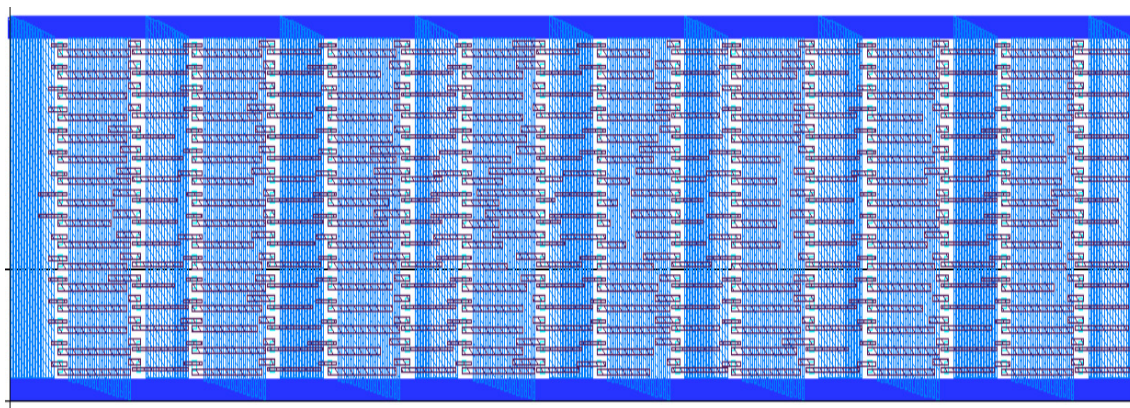


Figure 6.15: Generated DACs layout.

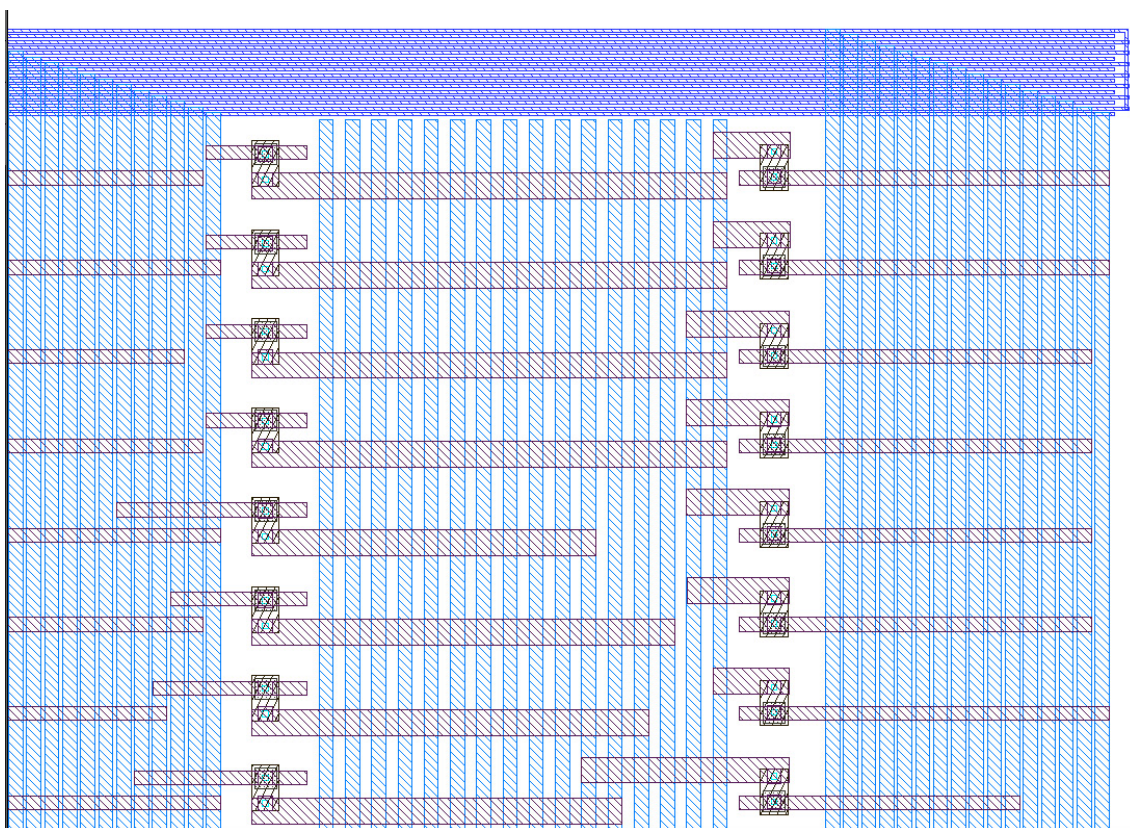


Figure 6.16: Routing of the generated MIM matrix.

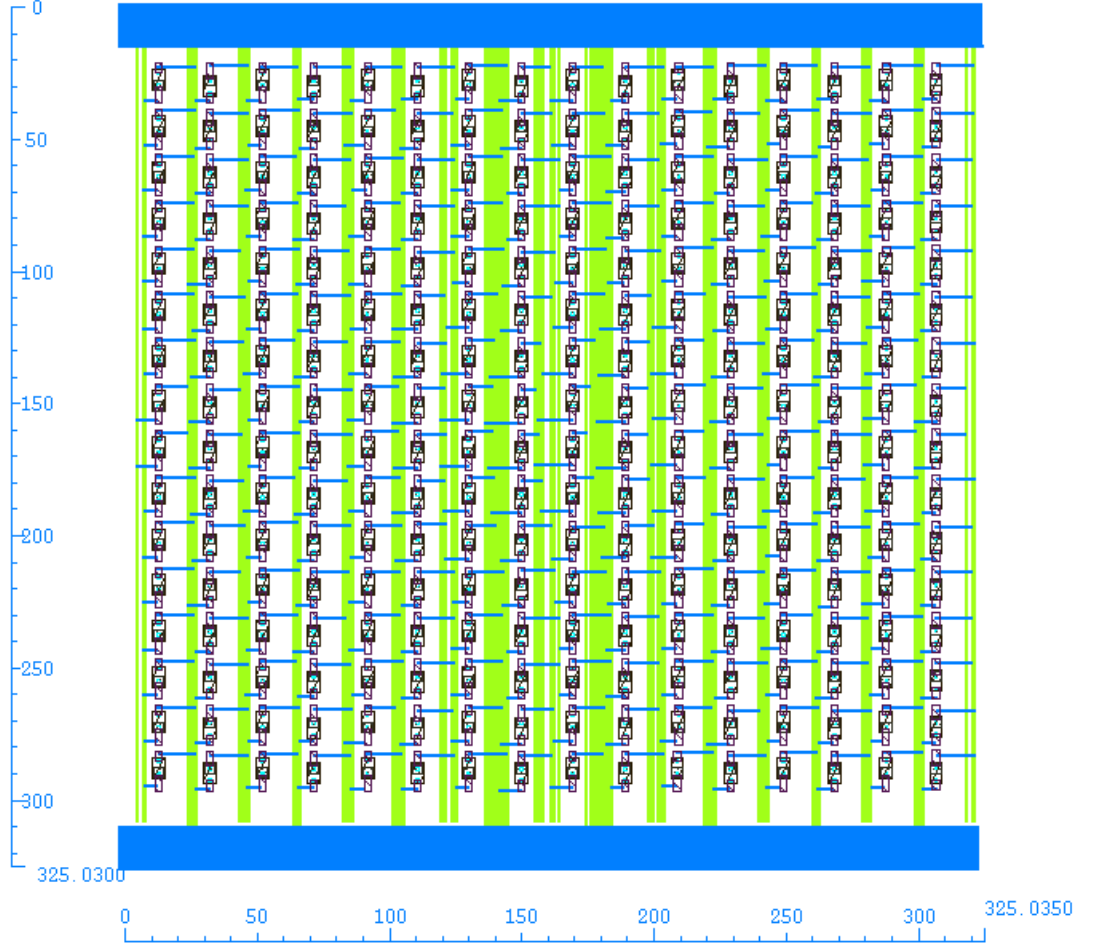


Figure 6.17: Modified DACs layout.

6.9 DAC Modified Layout

In order to overcome the disadvantages of the MIM-matrix generator, the matrix was rebuild and routed manually, metal 5 and metal 6 were used for routing as to minimize parasitics to the substrate. Metal 6 was used to tie the bottom and upper plates and metal 5 was used for the vertical paths. Each of the vertical paths corresponds to a terminal of one of the 16 capacitors made by the 256 units. Each vertical path collects the terminals of the units corresponding to its capacitor then again the top and bottom 16 horizontal paths of metal 6 collects the upper plates and bottom plates. The horizontal top paths made 2 terminals corresponding to the DACs outputs while those of bottom paths made the other 16 terminals of the capacitors to tie with the switches. The modified layout is shown in Fig.6.17 and a close look in Fig. 6.18 shows the area reduction due to routing with metal 5 and 6 besides the eliminated redundant paths.

The unused vertical paths were eliminated to help decrease routing parasitics besides routing with metal 6 and 5 didn't consume a huge area like the former approach and allowed a squared layout. The modified layout cut out the parasitics to ground to the third and the consumed area is $0.1056mm^2$. The inter-capacitance parasitics due to routing becomes negligible.

6.10 Performance Table

Table 6.3 compares the designed ADC performance with state-of-the-art realizations of low-power SA-ADC. The simulation results of this work were tabulated without adding the digital part contribution while the results of the other realizations in the comparison came from measurements of both digital and analog parts. The current FOM and power can be further decreased by the use of a smaller unit capacitance.

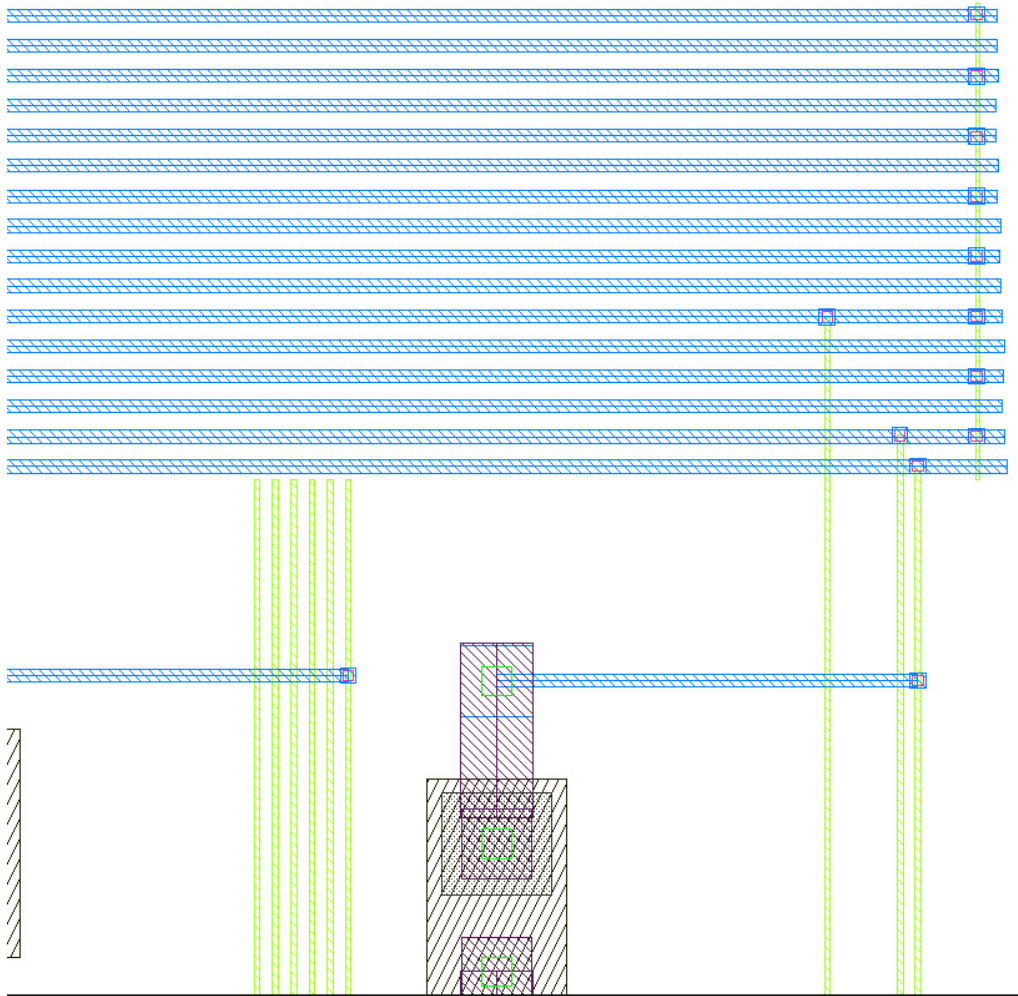


Figure 6.18: Routing of the modified layout.

Table 6.3: Performance comparison with State-of-the-art implementations.

Reference	Architecture	Tech. (μm)	C_u (fF)	F_s (KHz)	V_{dd} (V)	ENOB (bit)	ERBW (KHz)	Power (μW)	Area (mm^2)	FOM (pJ/step)
[Maloberti08][17]	SE-Double-Attenuator	0.18	120	100	1.0	9.4	50	3.8	0.24	0.056
[Hong07][9]	SE-Double	0.065	24	200	0.9	7.58	100	2.47	0.062	0.065
[This work] ¹	Diff-triple	0.13	30	111	1.2	7.6	55	0.722	0.122	0.033
[Verma06][18]	SE-Double	0.18	NA	100	1.0	10.55	50	25	0.63	0.166
[Scott03][1]	SE-Double	0.25	12	100	1.4	7.9	50	4.6	0.053	0.193

The attenuator method as in [17] or the reconfigurable radix method [16] are also good solutions to decrease the DAC consumption.

6.11 Conclusion

A systematic design case was studied. From system specifications, the unit capacitance was selected and the comparator specifications were defined. Minimal size switches were adequate for the target sampling frequency. Both a single-ended double-reference and a differential triple-reference architectures were designed. A comparator was designed for each architecture because of the different needed biasing. Power consumption was found to be $0.72\mu\text{W}$ per conversion neglecting the digital part. The verification plan used a set of transient analysis to characterize the static and dynamic performance of the ADC. The INL and DNL were within $\pm V_{LSB}/2$ with transistor level simulations while the SNDR recorded was 47.47 dB. Layout common centroid techniques were used for the comparator and the DAC generated layout. To solve the problems of huge parasitics and consumed area of the generated DAC, another manual layout was made. The new layout reduced the parasitics by 66% and the area by 68%.

¹Analog part simulation only

Conclusion and Perspectives

7.1 Conclusion

Today, many emerging applications, like cognitive radios and wireless sensor nodes demand low-power consumption rather than high resolutions. It leads to reviving moderate resolution and low-power converters like the successive approximation register (SA-ADC). Techniques like interleaving and asynchronous operation were proposed to enhance this ADC performance for wide bandwidth systems. The very low power consumption reported by state-of-the-art SA converters turned the topic to be one of the top research subjects in the last few years.

In this thesis, a systematic design methodology was presented for the successive approximation ADC from system specifications to layout. A general simulation environment was developed in VHDL-AMS allowing simulations with multiple abstraction levels. The system blocks were simulated using ideal models and BSIM3 models. The ADC performance was also characterized with different mismatch values introduced on the unit capacitances.

The different system architectures were analyzed and design trade-offs for the system blocks were discussed. The single-ended architecture suffers a possible leakage problem. Two solutions were then discussed to solve this problem, namely, the charge-pump and the bootstrap switches. Both were capable of solving the leakage problem but with further reliability problems. The charge-pump solution is limited to normal SAR algorithms and can not be used with arbitrary search algorithms while the bootstrap doesn't have this limitation. A modified bootstrap switch was proposed to solve the leakage problem while guarding switches reliability.

Tools developed in the LIP6 laboratory for analog design automation and reuse were utilized through the design cycle. The analog automated design tool COMDIAC was used for the comparator design. This analog synthesizer offers very accurate designs based on BSIM3 models. CAIRO language programs were then written for layout description. CAIRO layout description is independent of the technology. It turns the layout into a customizable program with a complete freedom to change the design parameters or the technology used without changing the layout.

To verify the proposed approach, a single-ended double-reference and differential triple-reference SA-ADC architectures were designed with the standard specifications for wireless sensor nodes.

- **Resolution:** 8bit
- **BW:** 50KHz
- **low-power**

The DAC topology used a binary weighted capacitors. A unit capacitance of $30fF$ was chosen with minimal switch sizes. A $1\mu A$ low-power comparator was designed. The comparator current path is cut through control switches during the reset phase to reduce power consumption. Both designs performances were adequate. Verifications were done with transient analysis, frequency analysis, tracing the signal-to-noise and distortion ratio with the input amplitude, input frequency and mismatch analysis. INL and DNL were verified within $\pm V_{LSB}/2$. The $SNDR_{max}$ is 47.44dB. The power consumption of the analog blocks is $\approx 0.72\mu W$ and the Figure of Merit is 0.033 pJ/bit

The differential architecture was implemented in technology ST 0.13 μm 1P6M with MIM capacitors. Special care was taken for mismatch in unit capacitance of the DAC which came on the account of increasing routing parasitics. For optimized matching, a C program was used to distribute a general number of capacitors on common centroid basis. The generated layout for the comparator passed parasitics extraction and post-simulation without performance degradation. The generated layout of the differential DACs had problems in terms of area and routing parasitics. The upper plate parasitics add an offset that can be removed in the digital domain while the bottom plate parasitics do not interfere with the ADC operations. The problematic parasitics are the routing inter-capacitor parasitics. Then a modified manual version was presented and successfully reduced the routing parasitics while the area was decreased to $0.1056mm^2$. The realized layouts passed successfully the DRC and LVS checks.

7.2 Perspectives

It is very interesting to extend the use of SA-ADC to the high frequencies while keeping its main advantages in low power consumption, reconfigurability and technology portability. Several techniques were reported in [30]-[15]-[16]-[5] in this purpose based on

- Interleaving
- Asynchronous operation
- Non-binary redundant codes

-
- Digital calibration.

At these frequencies the comparator and DAC as well as the control switches design and layout will be more challenging. The comparator kickback noise becomes more effective. Binary weighted capacitors will be no more suitable for the DAC and structures based on attenuator capacitor or the reconfigurable radix are needed to extend the system bandwidth. The drawback of these structures is their parasitic sensitivity. The layout and routing will be then more difficult. It will be very profitable to establish an automatic design tool for the SA-ADC at high frequencies, that receives from the designer the target specifications and the architecture. Then through the use of a set of functions like those offered by the tools we introduced in this thesis, it returns:

- The design based on multiple abstraction levels from behavioral to technology models
- The SA-ADC layout
- Verification for the performance parameters

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ملخص الرسالة

تزايد الاهتمام في السنوات الأخيرة بمحاولات الإشارة التناظرية الرقمية بتقنية التقريبات المتتابعة لخفض معدلات استهلاك الطاقة في نطاق عريض من أجهزة الاتصالات الحديثة. ويقدم هذا البحث طريقة نظامية لتصميم محول من هذا النوع من مستوى النظام الى الرسم التخطيطي على السليكون مع التركيز على تقنيات التصميم التناظري الألي. تم تصميم نموذجين على مستوى الترنزستور للبنية الأحادية والتفاضلية مع مقترحات لخفض استهلاك الطاقة و حل مشكلة تسريب الشحنات. تمت محاكاة النموذج بمواصفات شبكات المجسات اللاسلكية فائقة الصغر في تكنولوجيا 0.13 ميكرومتر بمعدل استهلاك 0.72 ميكرو وات و دقة فعلية 7.3 بيت مع التصميم على السليكون على مساحة 0.122 مم² بتكنيك المحور المركزي المشترك و قابلية اعادة الاستخدام مع أي تكنولوجيا.

(الكلمات الدالة: محاولات الإشارة ، التقريبات المتتابعة، المحور المركزي المشترك، شبكات المجسات اللاسلكية، التصميم التناظري الألي)

المحتويات

الباب الأول هو مقدمة عن متطلبات أجهزة الاتصالات الحديثة من احتياج لتوفير استهلاك الطاقة مع الاكتفاء بدقة متوسطة و أثر ذلك على تزايد الاهتمام بمحاولات الإشارة التناظرية الرقمية بتقنية التقريبات المتتابعة بالإضافة الى سرد أهداف الرسالة و محتوياتها.

الباب الثاني يستعرض الخطوات المتبعة أثناء عملية تحويل الإشارة كأخذ العينات والتكميم و تأثير كل منها على الشوشرة و الدقة الفعلية للمحول ثم يتعرض لأساليب تقييم أداء محولات الإشارة بشكل عام و ينتهي بمقارنة بين محولات الإشارة التناظرية الرقمية الحديثة القائمة على مبدأ نيكويست من حيث السرعة و استهلاك الطاقة.

الباب الثالث يتناول تقنية التقريبات المتتابعة من حيث التصميم على مستوى النظام فيبدأ باظهار مرونة التقنية و سهولة تغيير الدقة حسب التطبيق عن طريق البرمجة و بدون الحاجة الى أي تغيير على مستوى الترنزستور. يتبعها تصوير دقيق لعمليات النظام بالبنية التفاضلية و البنية الأحادية و مناقشة لمزايا و استخدامات البينيتين. ثم يختتم بنتائج المحاكاة على مستوى النظام مع رسم بياني لخوارزميات التحكم.

الباب الرابع يركز على تنفيذ جميع مكونات النظام على مستوى الترنزستور و يتعرض لتأثير الشوشرة و لا مثالية المكثفات والمفاتيح وكيفية اختيار القيم الملائمة للتصميم ثم يتطرق للعوامل المؤثرة على أداء المقارن و العناصر الأساسية في تصميمه. يطرح هذا الباب علاجاً لمشكلة تسريب الشحنات في البنية الأحادية باستخدام مفتاح مدعم بخاصية البوتستراب تم تعديله للحفاظ على إعتدالية الأداء للحد الأقصى.

الباب الخامس يقدم طريقة تصميم نظامي لمحول إشارة تناظري رقمي بتقنية التقريبات المتتابعة من مستوى النظام مروراً بمستوى الترنزستور وحتى الرسم التخطيطي على السليكون مع التركيز على استخدام تقنيات التصميم التناظري الألي. يدرس هذا الباب تأثير عدم التوافق بين وحدات المكثفات على زيادة الشوشرة عن طريق المحاكاة و يعرض طريقة لتوزيع وحدات المكثفات على السليكون بتكنيك المركز المتوسط المشترك.

الباب السادس يمثل دراسة حالة لنموذج بمواصفات شبكات المجسات فائقة الصغر فيمر بمراحل التصميم المختلفة حتى الرسم التخطيطي على السليكون. و يتم بعدها التحقق من الأداء عن طريق بيئة محاكاة تم انشاؤها لكي تستوعب بمرحلة نماذج مثالية أو حقيقية أو مختلطة مع عرض لعينات من نتائج المحاكاة و نتائج الرسم التخطيطي النهائي على السليكون. يختتم هذا الباب بمقارنة بين نتائج التصميم المقدم وبعض التصميمات الحديثة لذات المواصفات.

الباب السابع يشرح خلاصة الرسالة و محاور البحث المستقبلية الممكنة

تصميم نظامي لمحول اشارة تناظري- رقمي بتقنية التقريبات المتتابعة

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