

Vinod Pangracious

Curriculum Vitae

Education

- Since 2011 **Doctoral Student**, *Université Pierre et Marie Curie, Paris VI, Laboratoire LIP6, Paris France, .*
- Doctoral Thesis: *Development of a Stack-based 3D FPGA Demonstrator using 3D Technology Process. Expected to graduate by May 2014*
- Director: *Professor Habib Mehrez, LIP6/UPMC Paris (Habib.Mehrez@lip6.fr)*
- 1997–2000 **Masters of Technology (M.Tech)-Microelectronics**, *Indian Institute of Technology, Bombay, GPA – 8.8/10.*
- Masters Thesis: *Simulation and Modeling Hot Channel and Radiation Effects in MOS/SiGe HBT Devices: Modeling and characterization of surface and displacement damages in MOS and SiGe HBTs: Reference publication year 2000. Motorola USA sponsored scholarship, Partnership with Delft University Netherlands: Summer 2000 at Delft*
- Director: *Professor Juser M Vasi, EE Department IIT Bombay (jvasi@ee.iitb.ac.in)*
- 1991–1995 **Bachelor of Technology (B.Tech)-Electronics Engineering**, *Cochin University of Science And Technology, Kochi, GPA – 7.3/10, Specialized in Electronics And Communication.*
- Bachelor Thesis: *Design And Implementation of Digital Frequency Scanner for HAM Radio*

Selected Publications

- 2013 V Pangracious, Z Marrakchi, E Amouri, H Mehrez, **Performance Analysis and Optimization of High Density Tree-based 3D Multilevel FPGA**, *ARC 2013 LA USA, Reconfigurable Computing: Architectures, Tools and Applications*, 197-209
- 2013 V Pangracious, Z Marrakchi, H Mehrez, **Architecture Level TSV Count Minimization Methodology for 3D Tree-based FPGA**, *IEEE Cool Chips XVI Yokohama Japan (COOL Chips), 2013*
- 2013 V Pangracious, Z Marrakchi, H Mehrez, **Designing 3D Tree-based FPGA: Interconnect Optimization and Thermal Analysis**, *IEEE IC Design & Technology (ICICDT), 2013 International Conference on, 223-226, Pavia Italy*
- 2013 V Pangracious, Z Marrakchi, U Farooq, H Mehrez, **High Performance 3-Dimensional Heterogeneous Tree-based FPGA Architectures (HT-FPGA)**, *ACM FPGAWorld13, September 10 - 12 2013, Stockholm, Sweden*

- 2013 V Pangracious, Z Marrakchi, H Mehrez, **Designing a 3D Tree-based FPGA: Optimization of Butterfly Programmable Interconnect Topology Using 3D Technology**, *IEEE 3D System Integration Conference 2013 San Francisco USA*
- 2011 JL Ayala, A Sridhar, V Pangracious, D Atienza, Y Leblebici, **Through Silicon Via-based Grid for Thermal Control in 3D Chips**, *Nano-Net, 90-98, 2011 EPFL, Switzerland*
- 2000 J. Basak, A.T. Mahfooz, A. Mitra, V. Pangracious, L Nanver, A M Shaikh, J vasi, **Effect of Ionizing and Neutron Radiation on SiGe HBTs**, *Proceedings Int. Conf. on Communications, Computers and Devices (ICCCD-2000)*

Research Experience

- 2011–Present **Doctoral Research**, UNIVERSITÉ PIERRE ET MARIE CURIE, PARIS VI, PARIS, *Development of a Stack-based 3D FPGA Demonstrator using 3D Technology Process. 3D CAD tools development, Design and implementation 3D Tree-based FPGA demonstrator, reference publication 2013.*
- 2009–2010 **Research Associate**, ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE SWITZERLAND, *Design and Manufacturing of 5 tier 3D MPSoC emulation chip and validation of 3D resistance mesh-based Thermal Model, refer publication -2011.*

Industry Experience

- 2001–2004 **Staff Product Design Engineer:-Project Leader**, CYPRESS SEMICONDUCTOR INC USA, San Jose, Bangalore, India.
Responsible: Product Design and Characterization–Memory Product Division, Project Leader 130nm 16 and 32M SRAM design, Characterization and Technology Qualification
- 2004–2007 **Staff R & D Development Engineer**, INFINEON TECHNOLOGIES AG GERMANY, Dresden.
Research And Development Group: New Memory cell development using Capacitor over Bit line technology (Stack Capacitor)
- 2007–2009 **Sr Member of Technical Staff**, INNOVATIVE SILICON SA SWITZERLAND, EPFL Scientific Park Lausanne, Switzerland.
Responsibilities: Research And Development Group: Zero Capacitor memory (ZRAM) cell development using SOI technology (Single Transistor Memory Cell using floating body effect): Setup test and characterization laboratory for ZRAM development.

Teaching Experience

- 1996–1997 **Teaching Assistant**, NATIONAL INSTITUTE OF TECHNOLOGY, Calicut India.
Electronics Engineering Department: Handled undergrad courses (Semiconductor Devices, Circuits and Design) and Laboratory experiment class.
- 2010–2011 **Associate Professor**, RAJAGIRI SCHOOL OF ENGINEERING AND TECHNOLOGY, Kochi India, Electronics Engineering Department.
Responsibilities: Setup new Nanoelectronics system Laboratory: Lead semiconductor industry sponsored research projects. Handled courses for Undergrad and Master level programs: (VLSI Design and Technology). Worked as VLSI design course instructor at Wipro Technologies Kochi (www.wipro.com), a Master level professional orientation course for employees at VLSI Design group in collaboration with BITS Pilani (www.bits-pilani.ac.in).

*Université Pierre et Marie Curie, Paris VI, Laboratoire LIP6
4, Place Jussieu, 75252 Paris Cedex 05, France*

Awards

- 1997 Motorola USA Scholarship for Master program at IIT Bombay
1989 Gold Medalist: 1st Rank at 10th Grade: Craven LMS High School Kollam, India

Languages

English	Advanced	
Malayalam	Mothertongue	
German, Tamil, Hindi	Intermediate	<i>Conversationally fluent</i>
French	Basic	<i>Basic words and phrases only</i>

Personal Contact

Address	417,Maison De L'Inde, 7R Boulevard Jourdan, Paris 7514.	
Email1	Vinod.Pangracious@etu.upmc.fr, Vinod.Pangracious@lip6.fr	<i>official</i>
Email2	pangracious@gmail.com	<i>private</i>
Phone	+33 6 46 20 30 96	<i>mobile</i>

Referrals

- Reference 1 **Zied Marrakchi**
Title **CTO, Flexras Technologies**
Address **153 Boulevard Anatole France 93200 Saint-Denis, Paris France**
Email **zied.marrakchi@flexras.com**
- Reference 2 **Habib Mehrez**
Title **Professor, Université Pierre et Marie Curie,Paris VI, Director CIAN/LIP6**
Address **4, Place Jussieu, 75252 Paris Cedex 05, France.**
Email **Habib.Mehrez@lip6.fr**
- Reference 2 **Emna Amouri**
Title **Post Doc at Telecom Paris-Tech, Comelec Department**
Address **46 Rue Barrault, 75634 Paris Cedex 13**
Email **emna.amouri@telecom-paristech.fr**